NIST SPECIAL PUBLICATION 400-97

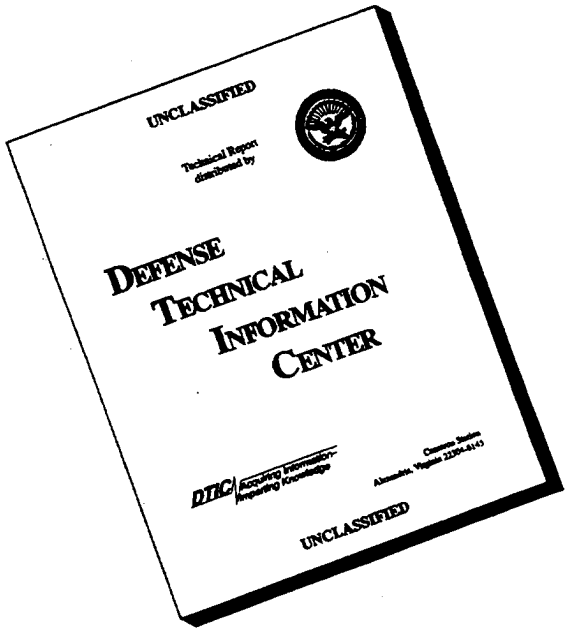
U.S. DEPARTMENT OF COMMERCE/Technology Administration
National Institute of Standards and Technology

Semiconductor Measurement Technology:

Test Structure Implementation Document: DC Parametric Test Structures and Test Methods for Monolithic Microwave Integrated Circuits (MMICs)

C. E. Schuster

DISCLAIMER NOTICE



THIS DOCUMENT IS BEST QUALITY AVAILABLE. THE COPY FURNISHED TO DTIC CONTAINED A SIGNIFICANT NUMBER OF PAGES WHICH DO NOT REPRODUCE LEGIBLY.

The National Institute of Standards and Technology was established in 1988 by Congress to "assist industry in the development of technology . . . needed to improve product quality, to modernize manufacturing processes, to ensure product reliability . . . and to facilitate rapid commercialization . . . of products based on new scientific discoveries."

NIST, originally founded as the National Bureau of Standards in 1901, works to strengthen U.S. industry's competitiveness; advance science and engineering; and improve public health, safety, and the environment. One of the agency's basic functions is to develop, maintain, and retain custody of the national standards of measurement, and provide the means and methods for comparing standards used in science, engineering, manufacturing, commerce, industry, and education with the standards adopted or recognized by the Federal Government.

As an agency of the U.S. Commerce Department's Technology Administration, NIST conducts basic and applied research in the physical sciences and engineering, and develops measurement techniques, test methods, standards, and related services. The Institute does generic and precompetitive work on new and advanced technologies. NIST's research facilities are located at Gaithersburg, MD 20899, and at Boulder, CO 80303. Major technical operating units and their principal activities are listed below. For more information contact the Public Inquiries Desk, 301-975-3058.

Office of the Director
- Advanced Technology Program
- Quality Programs
- International and Academic Affairs

Technology Services
- Manufacturing Extension Partnership
- Standards Services
- Technology Commercialization
- Measurement Services
- Technology Evaluation and Assessment
- Information Services

Materials Science and Engineering Laboratory
- Intelligent Processing of Materials
- Ceramics
- Materials Reliability[1]
- Polymers
- Metallurgy
- Reactor Radiation

Chemical Science and Technology Laboratory
- Biotechnology
- Chemical Kinetics and Thermodynamics
- Analytical Chemical Research
- Process Measurements
- Surface and Microanalysis Science
- Thermophysics[2]

Physics Laboratory
- Electron and Optical Physics
- Atomic Physics
- Molecular Physics
- Radiometric Physics
- Quantum Metrology
- Ionizing Radiation
- Time and Frequency[1]
- Quantum Physics[1]

Manufacturing Engineering Laboratory
- Precision Engineering
- Automated Production Technology
- Intelligent Systems
- Manufacturing Systems Integration
- Fabrication Technology

Electronics and Electrical Engineering Laboratory
- Microelectronics
- Law Enforcement Standards
- Electricity
- Semiconductor Electronics
- Electromagnetic Fields[1]
- Electromagnetic Technology[1]
- Optoelectronics[1]

Building and Fire Research Laboratory
- Structures
- Building Materials
- Building Environment
- Fire Safety
- Fire Science

Computer Systems Laboratory
- Office of Enterprise Integration
- Information Systems Engineering
- Systems and Software Technology
- Computer Security
- Systems and Network Architecture
- Advanced Systems

Computing and Applied Mathematics Laboratory
- Applied and Computational Mathematics[2]
- Statistical Engineering[2]
- Scientific Computing Environments[2]
- Computer Services
- Computer Systems and Communications[2]
- Information Systems

[1]At Boulder, CO 80303.
[2]Some elements at Boulder, CO 80303.

Semiconductor Measurement Technology:

Test Structure Implementation Document: DC Parametric Test Structures and Test Methods for Monolithic Microwave Integrated Circuits (MMICs)

C. E. Schuster

Semiconductor Electronics Division
Electronics and Electrical Engineering Laboratory
National Institute of Standards and Technology
Gaithersburg, MD 20899-0001

Sponsored by:
Defense Advanced Research Projects Agency
Arlington, VA 22209-2308
and
U.S. Air Force Wright Laboratory
Wright-Patterson AFB, OH 45433-6543

September 1995

U.S. DEPARTMENT OF COMMERCE, Ronald H. Brown, Secretary
TECHNOLOGY ADMINISTRATION, Mary L. Good, Under Secretary for Technology
NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY, Arati Prabhakar, Director

National Institute of Standards and Technology Special Publication 400–97
Natl. Inst. Stand. Technol. Spec. Publ. 400–97, 85 pages (September 1995)
CODEN: NSPUE2

U.S. GOVERNMENT PRINTING OFFICE
WASHINGTON: 1995

For sale by the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402–9325

TABLE OF CONTENTS

Page

ABSTRACT 1
Key Words 1
EXECUTIVE SUMMARY 2

1. INTRODUCTION 5
1.1. Purpose 5
1.2. Scope 5
1.2.1. NISTGAAS Form and Function 5
1.2.2. Documentation 5

2. IMPLEMENTATION CONSIDERATIONS 6
2.1. Selecting Test Structures 6
2.2. Developing a Test Vehicle 8
2.3. Assuring the Testing Environment 9
2.4. Developing Data Analysis Capabilities 9

3. COMPUTER-AIDED DESIGN (CAD) CELL LIBRARY 9
3.1. Overview 9
3.2. Process Layers 10
3.3. Plot Colors and Patterns 10
3.4. Cell Naming Conventions 10
3.4.1. Test Structure Names 12
3.4.2. Layer Names 12
3.4.3. Dimensions 13
3.5. CAD Drawing Hierarchy 13
3.6. Obtaining the NISTGAAS Cell Library 13

4. ACKNOWLEDGMENTS 14

5. REFERENCES 14

APPENDICES

Appendix A - NISTGAAS Cell Library Contents 15
A.1 List of Test Structures 17
A.2 Library Hierarchy 17
A.3 Process Layer Designators 17
A.4 Cell Contents 17
Appendix B - NISTGAAS Test Structure Specification 23
B.1 Kelvin-Cross Interfacial Contact Resistor (Four-Pad) 27
B.2 Kelvin-Cross Interfacial Contact Resistor (Shared-Pad) 33
B.3 Nanometer-Resolution Electrical Alignment Structure 41
B.4 Mesa/Channel van der Pauw Sheet Resistor 51
B.5 Step Coverage/Interconnect Meander 57
B.6 Interconnect Resistor 61
B.7 Cross-Bridge Resistor 65
B.8 MIMIC-Standard 200 μm FET 71
Appendix C - NISTGAAS Test Structure Sideviews 79

LIST OF FIGURES

Page

Figure 1. Selecting Test Structures and Test Vehicles 7
Figure 2. Fabrication Process Steps 11
Figure A-1. NISTGAAS Top-Level CAD Drawing 20
Figure A-2. NISTGAAS 2nd-Level CAD Drawing 21
Figure C-1. Sideview: Kelvin-Cross Interfacial Contact Resistor (Four-Pad) 81
Figure C-2. Sideview: Kelvin-Cross Interfacial Contact Resistor (Shared-Pad) 82
Figure C-3. Sideview: Nanometer-Resolution Alignment Structure 83
Figure C-4. Sideview: Mesa/Channel van der Pauw Sheet Resistor 84
Figure C-5. Sideview: Step Coverage/Interconnect Meander 85
Figure C-6. Sideview: Interconnect Resistor 86
Figure C-7. Sideview: Cross-Bridge Resistor 87
Figure C-8. Sideview: MIMIC-Standard 200 µm FET 88

LIST OF TABLES

Page

Table 1. NISTGAAS Cell Types and Their Application 3
Table 2. NISTGAAS Design Rules 10
Table A-1. NISTGAAS Test Structures and CAD File Locations (Page 1 of 2) 18
Table A-2. Mapping of Color/Pattern to Process Layer 22

LIST OF SCHEMATICS

Page

Figure B-1. Kelvin-Cross Interfacial Contact Resistor (Four-Pad) 29
Figure B-2. Kelvin-Cross Interfacial Contact Resistor (Shared-Pad) 34
Figure B-3. Nanometer-Resolution Electrical Alignment Structure (Horizontal) 43
Figure B-4. Nanometer-Resolution Electrical Alignment Structure (Vertical) 44
Figure B-5. Mesa/Channel van der Pauw Sheet Resistor 52
Figure B-6. Step Coverage/Interconnect Meander 58
Figure B-7. Interconnect Resistor 62
Figure B-8. Cross-Bridge Resistor 66
Figure B-9. MIMIC-Standard 200 µm FET (Horizontal) 72
Figure B-10. MIMIC-Standard 200 µm FET (Vertical) 73

Semiconductor Measurement Technology:

Test Structure Implementation Document: DC Parametric Test Structures and Test Methods for Monolithic Microwave Integrated Circuits (MMICs)

C. E. Schuster

Semiconductor Electronics Division
National Institute of Standards and Technology
Gaithersburg, MD 20899

ABSTRACT

This document describes a set of microelectronic test structure designs for manufacturers of GaAs MMIC devices. These designs enable the dc measurement of process and device parameters that can be used to diagnose, monitor, compare, and predict the performance of the fabrication process or the devices produced. The test structure designs are embodied in a computer-aided design library known as NISTGAAS, which contains 8 types of test structures, implemented in 125 combinations of process layer and size, and based on a 2 x 6 probe-pad array. Any design, once fabricated on a wafer, can be probed using commonly available commercial parametric test system equipment. This document specifies how to implement and test each type of test structure and how to analyze the results. It also provides guidance on how to apply the set of test structures at the wafer level. Although NISTGAAS was designed for the process described in this document, it was also designed and demonstrated to be adaptable for other MMIC processes. Since NISTGAAS contains cell designs rather than a chip design, it provides a flexible test structure methodology that also provides the MMIC community with a common reference point for assessing process and device performance.

Key Words: CAD cell library; GaAs; integrated circuit; MMIC; parametric test method; process control; test structure

DISCLAIMERS

Certain commercial and public-domain products are identified to specify the procedures described in this document. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that the products identified are necessarily the best available for the purpose.

EXECUTIVE SUMMARY

The NISTGAAS computer-aided design (CAD) cell library was initially developed as part of the Defense Advanced Research Projects Agency (DARPA)/Tri-Service effort known as the Microwave/Millimeter Wave Monolithic Integrated Circuits (MIMIC) Program. The NISTGAAS library includes designs developed by NIST and the U.S. Air Force, Wright Laboratory (WL). The NISTGAAS development and validation were funded in part by WL MIPR Nos. FY1123-90-N9514, FY1175-91-N9518, FY1123-92-N9520, and FY1175-93-N9519.

Under the MIMIC Program, DARPA sponsored contracts for processes, products, and services to develop high-performance, affordable, and available microwave and millimeter-wave technology for manufacturing electronic systems. One aspect of this program was the Materials/Devices Correlation task (MIMIC Phase 1, Task 4.E), to investigate and quantify GaAs process performance through the use of test structures.

Six contractor foundries participated in Task 4.E, using test structures provided by WL. A common test chip, replicated about 200 times on each 3-inch wafer, was used by each contractor to produce high-density test structure data for 6 lots of 4 wafers each. Test structure data from the contractors and WL were analyzed by WL, with NIST assistance. Most test structures performed adequately for most process lots and lines. Some observations about performance variations provided guidance for improved test structure designs, test procedures, and test procedure specifications [1].

A second-generation wafer-level test vehicle, known as the High-Density Test Reticle (HDTR), was designed (partly) to investigate new test structure designs intended to improve and extend the performance of particular Task 4.E test structures and of the general test structure methodology. The HDTR test structures were designed by WL and NIST, fabricated by WL, and tested by WL and NIST [2, 3]. The HDTR test structures and other NIST test structure designs are contained in the NISTGAAS library, which includes the eight test structure types shown in Table 1. These types are implemented in 125 layer and size combinations, where each combination is a cell in the NISTGAAS library.

The NISTGAAS library and this implementation document provide the GaAs-based microwave community with a readily available, thoroughly documented, and flexible implementation method to use as a common reference point for assessing process and device performance.

Table 1. NISTGAAS Cell Types and Their Application

TEST STRUCTURE TYPES	APPLICATION
Kelvin-Cross Interfacial Contact Resistor (Four-Pad)	Determine interfacial contact resistances to assess quality of a contact type
Kelvin-Cross Interfacial Contact Resistor (Shared-Pad)	Determine interfacial contact resistances to assess quality of a contact type
Nanometer-Resolution Electrical Alignment Structure	Determine placement of a feature relative to two reference features to assess the performance of lithography processes/tools
Mesa/Channel van der Pauw Sheet Resistor	Determine sheet resistance of mesa and channel, thickness of channel to assess potential FET performance
Step Coverage/Interconnect Meander	Determine current continuity to assess step coverage for two conducting layers
Interconnect Resistor	Determine load resistance of a contact type to provide circuit design parameter
Cross-Bridge Resistor	Determine sheet resistance and linewidth to assess the quality of a conducting layer
MIMIC-Standard 200 μm FET	Determine dc FET parameters to assess FET performance

1. INTRODUCTION

1.1. Purpose

This document describes how to implement the test structures included in the NISTGAAS cell library. It specifies each test structure design, how to test it, and how to analyze the results. It also addresses how to apply the set of NISTGAAS test structures at the wafer level.

1.2. Scope

1.2.1. NISTGAAS Form and Function

The NISTGAAS cell library contains dc parametric test structures designed for a MMIC process that has design rules typical for fabricating 1 μm, low-noise, depletion-mode devices. The library can be used with other MMIC processes, as it is designed so the test structures can be easily customized for processes with similar but different design rules and mask layers. The CAD software used to create NISTGAAS is the (public-domain) Magic graphic layout editor [4], so the mask-level layout information for the test structure designs is transferable in either Caltech Intermediate Form (CIF) or Calma Stream format. Each test structure design can be tested using a dc parametric test system with a probe card that can access a 2 x 6 probe-pad array, where the probe pads are 75 μm x 75 μm each and have a 125 μm pitch.

Since the NISTGAAS library provides individual test structure designs (cells), rather than a test chip, only the designs useful for a particular application need be implemented. This enables the user to develop a flexible monitoring capability without sacrificing area (to non-applicable parts of a test chip), when such area might be better used for product or for design development.

1.2.2. Documentation

Each test structure type is specified in terms of its purpose, application, design variations, CAD, layout constraints, measurement method, computation and interpretation of results, and historical references. These specifications are found in Appendix B, while the remaining document provides information needed to understand and effectively use Appendix B.

This document is organized to provide adequate information for various types of users but to minimize the effort each needs to find details of interest or reproduce working-level aids.

Potential users include program managers, process engineers, CAD personnel, tester code developers, and data analysts. Generally applicable background information is in section 2 (general perspective on test structure implementation) and in section 3 (specific rationale, assumptions, and conventions used in designing the NISTGAAS cell library). Appendix A (library configuration) will be the most useful to CAD personnel. Appendix B (the test structure specifications) is intended mainly for coders and analysts, but can also be useful to program managers and process engineers in assessing the process-related aspects of test structure design and implementation. Process engineers may also find Appendix C (process sideviews) a useful extension to the Appendix B checkplots.

2. IMPLEMENTATION CONSIDERATIONS

To gain the maximum benefit from using test structures, users need to be conscientious not only in applying the specifications in Appendix B, but also in several other areas: selecting test structures, developing an appropriate test vehicle, assuring the testing environment, and developing data analysis capabilities. These areas are discussed in detail elsewhere [5] and here within the context of MMIC manufacturing environments and the NISTGAAS cell library. The sections on selecting test structures and test vehicles are summarized in figure 1.

2.1. Selecting Test Structures

As the first step in the test structure implementation process, the user should determine why test structures are needed – both broadly and specifically. In doing this, the expertise of process and design engineers is valuable. The reasons for using test structures affect the data needed and the test structures and test vehicle design to be used. The major consideration involves whether the test structures will be used to monitor a well-controlled production environment, to diagnose a new process, to develop process models, or to provide data for comparison to data from other process lines.

In a well-controlled process, the physics and the yield goals of the process and products are understood, so the critical parameters needed to monitor the process are well known and limited. In the other process environments and applications, many more parameters may be needed to develop correlations between process parameters or between process parameters and device parameters or to compare the capabilities of different process lines. These considerations affect not only which test structure types are needed, but also what layer/size combinations are needed.

In comparing data from different process lines, a common set of test structures, appropriate for all processes, is needed. If one of the common test structures has not previously been used on a process line, a line-specific test structure providing similar parameters should be retained to correlate process conditions based on previous history.

The layer/size combinations selected should be those actually used in the device or process step for which the test structure parameter is needed. If devices require features larger than the minimum size, designs with the same size features should be included. For example, to assess a FET with a 10 μm channel width, the mesa/channel van der Pauw is implemented with a 10 μm vs 4 μm linewidth. In determining a load resistance for the source or drain of a FET, a corresponding-size, ohmic-to-mesa interconnect resistor is used.

Further, particular process sensitivities may affect the choice of the NISTGAAS cell to be used. For example, if ohmic sheet resistance is adequately controlled but does vary, test structures with ohmic runs long enough to be susceptible to such variations should not be used. For the alignment structure, such a sensitivity could be minimized by using the OG vs GO cell.

Another consideration in selecting test structures involves how a mask set will be developed and used. By including designs with linewidths smaller than the process currently supports,

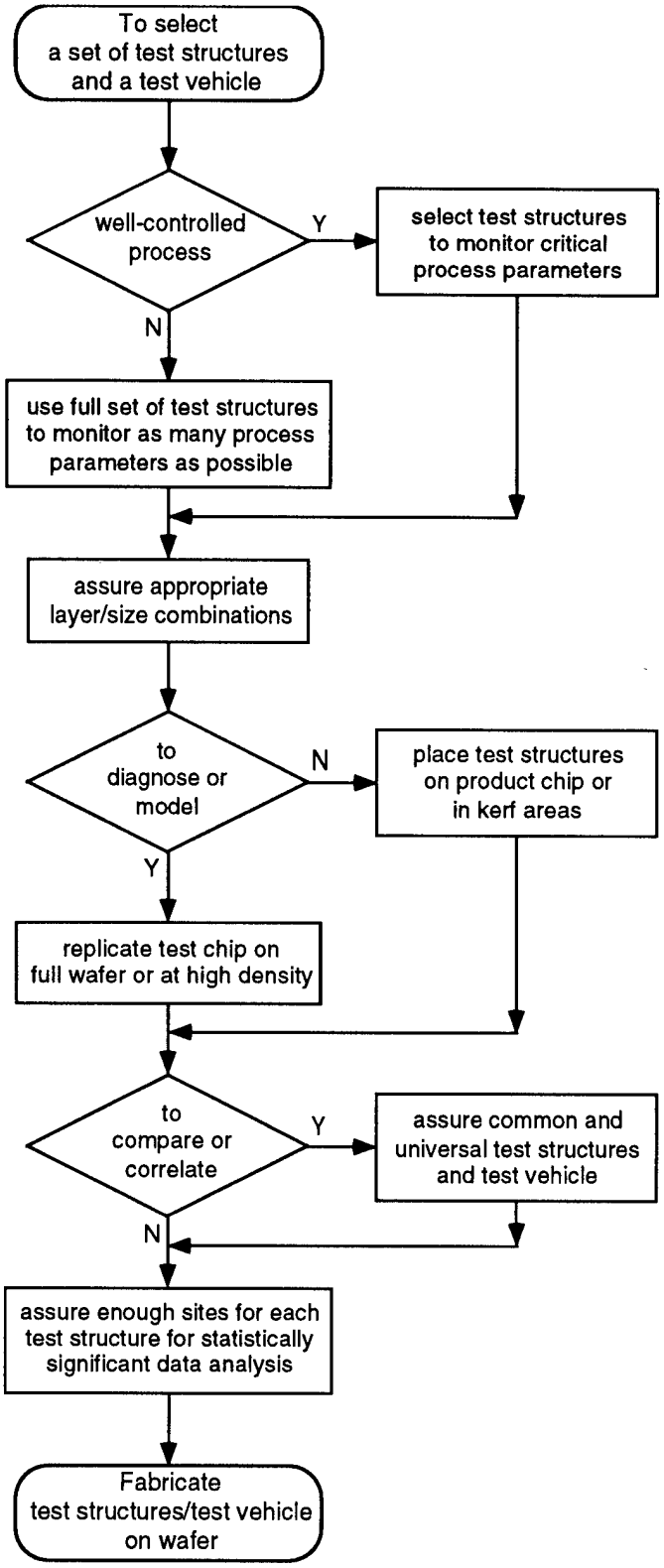


Figure 1. Selecting Test Structures and Test Vehicles.

the design limits of the process may be assessed and a new mask set is not needed for the next generation of the process. Such decisions are a trade-off with other factors such as test vehicle size and the cost, time, and needs associated with a new mask set.

2.2. Developing a Test Vehicle

Once the necessary test structure types and layer/size combinations are identified, the test vehicle implementation and layout can be developed. As in choosing test structures, a major consideration in test vehicle design is its application, e.g., to monitor, diagnose, model, or compare. Again, process and product design expertise is needed.

For process diagnosis and modeling, a full-wafer or other high-density test vehicle is needed to provide robust statistics for correlation and wafer-mapping analyses. Frequently, all of the test structures are included on a test chip that is replicated on an entire wafer or at a high density and uniformly distributed with product-related chips on a wafer. For monitoring a well-controlled and well-characterized process, reduced implementations that fit on the product chip or wafer or in the kerf area are usually adequate. Possible implementations are usually strip-like and known by such terms as test strip, coupon, pellet, or plug-bar.

Regardless of the test vehicle type, several layout factors are important. Most important is that the test structures should be located near the MMIC they are to characterize. Thus, a test chip implementation should either contain on-chip MMIC devices or have the salient test structures near the edge of the test chip that will be adjacent to the edge of a product chip with a near-by device. Similarly, test strips should have their test structures arranged to be near the related device. For example, if gate-to-ohmic alignment is critical for a FET, the gate-to-ohmic alignment structure should be located near a sample of the FET.

Another layout consideration is whether correlation between the test structure parameters is needed. The user must then decide which test structures need to be placed near each other and assure that their relation to near-by device needs are maintained.

Each test structure design should be replicated at sites that are uniformly distributed on the wafer. This provides some indication of parameter uniformity, the sites needed to perform the preliminary validation procedures included in some of the test structure specifications, and the sites needed to demonstrate data reproducibility. Although five sites are often used, this is about half the sites usually needed to provide a robust statistical basis for data analysis [6].

If comparisons between process lines are needed, a standard test vehicle with moderate to high density is usually needed. In addition to the above factors, this test vehicle must be designed to be accommodated by all the process lines. Process lines should consider retaining previously used process-specific test vehicles to correlate new parameters to previous history.

If adequate space is not available for the initially identified set of test structure designs, the set must be prioritized according to which designs provided the most useful information. This exercise should consider not only test structure type but also layer and size choices. For example, in assessing the quality of the different contacts in the process, having 3 vs 5 linewidths for all types of contacts may be preferable to having 5 linewidths for fewer types.

2.3. Assuring the Testing Environment

Before collecting data that will be analyzed for significant purposes, the hardware and software in the testing environment must be thoroughly validated. Instruments should be calibrated, the switching matrix and probe card connections verified, and other tester diagnostics performed. Software function and correct data logging should be demonstrated using known artifacts or benchmarks. This should verify that correct currents or voltages are forced or measured and that sufficient settling times are allowed to produce realistic results that are accurately stored in the intended locations in a database.

These activities are simply good engineering practice. Other assurances that relate more to specific measurement procedures for MMIC environments and NISTGAAS test structures are discussed in the introductory notes in Appendix B.

2.4. Developing Data Analysis Capabilities

Automated techniques with analyst-friendly interfaces should be developed to assure consistency in analyzing test structure data of more than minimal volume. The first step of such automation should include an algorithm to assure that measurements are reproducible. If the measurements are not reproducible, the cause needs to be determined, the problem resolved, and the measurements repeated. If measurements are reproducible, the next step should include a robust outlier exclusion algorithm, such as in reference [7], to remove data points that will skew further statistical analysis. Once reproducibility is demonstrated and outliers are excluded, the integrity of the data is sufficient to support further analysis. Some mechanism should also exist so that analysts can easily distinguish the original data from data that have successfully completed these evaluations.

3. COMPUTER-AIDED DESIGN (CAD) CELL LIBRARY

3.1. Overview

The NISTGAAS cell library was designed using the Magic CAD layout editor (version 6.3 on a Sun SPARCsystem 300 with SunOS 4.1.2 and Open Windows 2.0). The library layout and its associated technology file are designed in a hierarchical manner. The test structures are designed with constraints intended to assure portability and immunity to yield-limiting defects. These features enable the library to be customized easily for different mask layers and design rules. Because the library is hierarchical by test structure type and a cell naming convention is used, test structure designs are easily located and the framework for adding customized designs is available and obvious.

For most test structure types, a number of design variations are provided. The variations for a given test structure type result from different combinations of process layers and dimensions, producing a set of unique designs for that test structure type. Each design variation is a "cell" in the NISTGAAS library and is stored as a separate file within the library file hierarchy.

All the design variations for each test structure type are listed in Appendix A and are referenced in the specification for each test structure type in Appendix B. Although each specification shows the drawing for only one of the available cells, all cells referenced in the specification are found in the electronic version of NISTGAAS. To understand the NISTGAAS cell designs, some background process- and library-related information is needed.

3.2. Process Layers

The NISTGAAS technology file represents a common Metal-Semiconductor Field Effect Transistor (MESFET) process, where the design rules and processing steps support a planar process fabricating 1 μm, low-noise, depletion-mode devices. The design rules are summarized in table 2, and the processing steps are summarized in figure 2.

Table 2. NISTGAAS Design Rules

	M	O	R	G	M1	DI	AIR	T
Minimum width (μm)	4	4	4	1	1	4	4	4
Minimum space (μm)	5	4	4	2	2	4	4	4

where:

M = mesa
O = ohmic
R = resistor
G = gate
M1 = first metal
DI = dielectric (nitride)
AIR = air bridge
T = thick metal

3.3. Plot Colors and Patterns

Each process layer or construct in a cell is represented as a color, in the electronic format of NISTGAAS, and as a black and white pattern in the drawings in Appendix B. In the electronic version, a legend shows each layer name and the associated color. When the NISTGAAS cells are viewed on a Sun system or in black and white, the colors and patterns equate to the process layers and constructs as indicated in Appendix A.

3.4. Cell Naming Conventions

Cell names consist of two or three fields concatenated with the character "_" between each. The three fields include test structure name, layer name, and dimension. A description of each field follows, along with its valid entries.

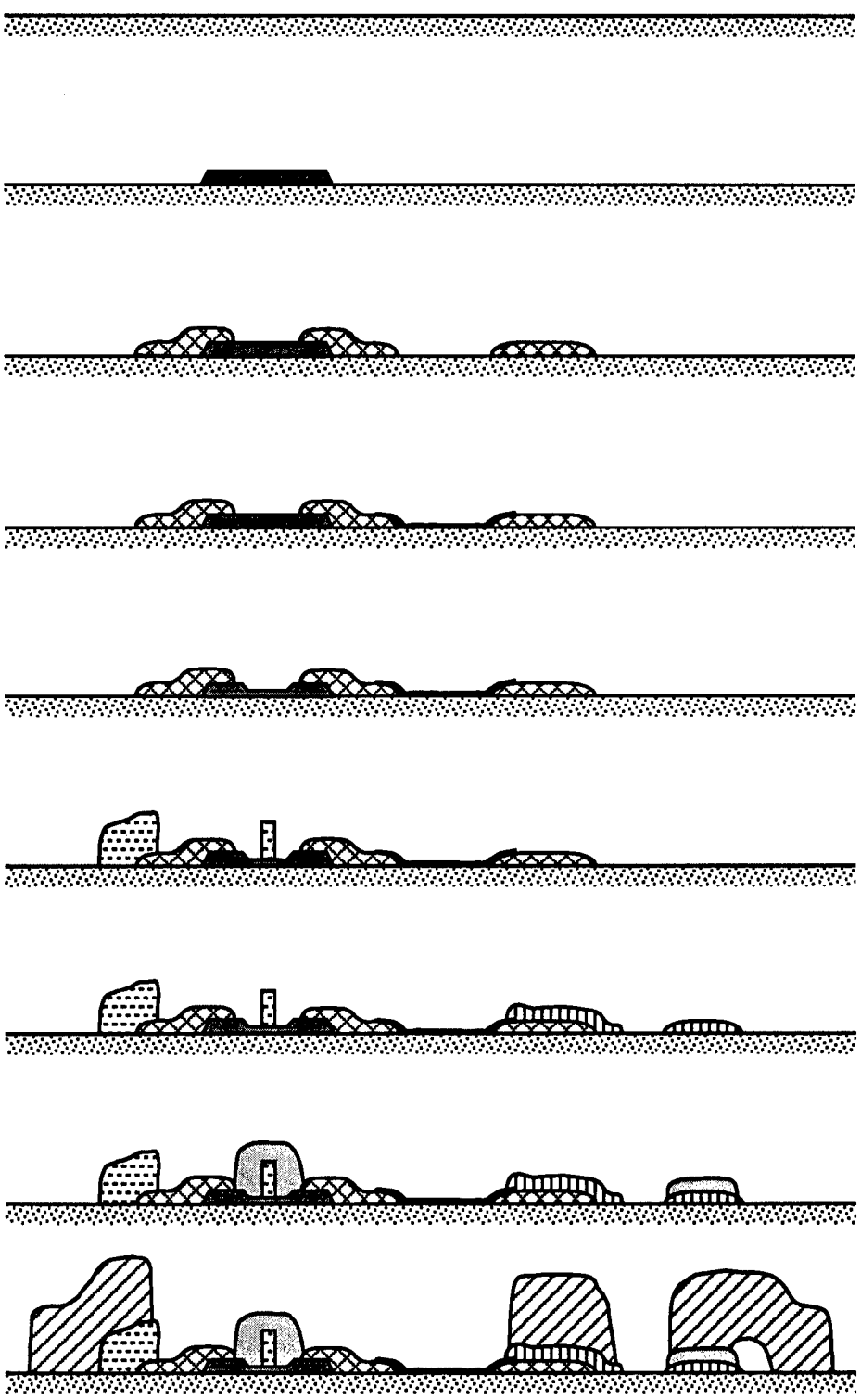


Figure 2. Fabrication Process Steps.

3.4.1. Test Structure Names

The test structure name field is an abbreviation of the full test structure name:

1. CONRES - Kelvin-Cross Interfacial Contact Resistor (Four-Pad)
2. CONRESSH - Kelvin-Cross Interfacial Contact Resistor (Shared-Pad)
3. ALIGNH and ALIGNV - Nanometer-Resolution Electrical Alignment Structure; names denote different designs for horizontal and vertical orientations
4. VPAUW - Mesa/Channel van der Pauw Sheet Resistor
5. MEANDER - Step Coverage/Interconnect Meander
6. INTRES - Interconnect Resistor
7. CROSSBR - Cross-Bridge Resistor
8. RFFETH and RFFETV - MIMIC-Standard 200 μm FET; names denote different horizontal and vertical designs based on the Task 4.E MESFET designs with the same names.

3.4.2. Layer Names

The layer name field identifies the process layer(s) in the test structure design. In most cases, a layer is indicated by its first letter, and multi-character layer names indicate two layers, with the upper layer occurring first in the layer name. The exceptions are: M1; AIR; and names noted as "in CONRESSH," where the name indicates which layer in the two sets of layers in the test structure is shared at pads used by both designs. The NISTGAAS layer names are:

1. M - mesa
2. O - ohmic; in CONRESSH: layer shared by OM and M1O designs
3. R - resistor; in CONRESSH: layer shared by RO and M1R designs
4. G - gate
5. M1 - first metal; in CONRESSH: layer shared by M1G and TM1 designs
6. T - thick metal; in CONRESSH: layer shared by TO and TG designs
7. AIR - air bridge (thick metal-dielectric-first metal)
8. OM - ohmic-to-mesa
9. RO - resistor-to-ohmic
10. GO - gate-to-ohmic
11. M1O - first metal-to-ohmic
12. TO - thick metal-to-ohmic
13. M1R - first metal-to-resistor
14. M1G - first metal-to-gate
15. TG - thick metal-gate
16. TM1 - thick metal-to-first metal

3.4.3. Dimensions

These represent dimensions in the test structure design, in micrometers: the width of a square contact or a bridge, or the dimensions of a FET gate. The NISTGAAS dimensions include:

1. 1
2. 2
3. 3
4. 4
5. 6
6. 8
7. 10
8. 12
9. 1x200

Thus, some typical cell names are VPAUW_M_4, CONRES_M1R_12, MEANDER_AIR, and RFFETH_1x200. For a complete list of the cell names for all of the NISTGAAS designs, see Appendix A.

3.5. CAD Drawing Hierarchy

The NISTGAAS cell library is hierarchical, with like cells grouped together. The library configuration is shown in Appendix A, which also describes how to navigate through the hierarchy to any test structure design.

3.6. Obtaining the NISTGAAS Cell Library

To obtain the NISTGAAS cell library and its associated technology file, or for more information, please contact:

C. E. Schuster
NIST
Bldg 225/Rm B360
Gaithersburg, MD USA 20899-0001

Phone: 1-301-975-2241
e-mail: schuster@sed.eeel.nist.gov

4. ACKNOWLEDGMENTS

The efforts of these individuals are notable in developing the NISTGAAS cell library and are appreciated: P. Roitman for guidance on designing the CAD library; R. A. Allen, for guidance on designing and testing the electrical alignment test structure; J. C. Marshall for developing the Magic technology file; C. H. Ellenwood for digitizing and managing the CAD library; and L. W. Linholm for many helpful comments. The NIST team also thanks WL personnel for their contributions: M. Mah for providing process information; D. Via for digitizing the MIMIC-Standard 200 μm FET; J. K. Gillespie and S. E. Cummins for providing test information for the MIMIC-Standard 200 μm FET, as well as many other helpful technical discussions; and, especially, R. T. Kemerley for encouraging and supporting the concept of a CAD cell library for MMIC test structures.

5. REFERENCES

[1] Schuster, C. E., Linholm, L. W., and Gillespie, J. K., High-Density Test Structures for Assessing Microwave/Millimeter Wave Monolithic Integrated Circuit (MIMIC) Performance, Digest of Papers, 1991 Government Microcircuit Applications Conference, Orlando, FL, November 5-7, 1991, Vol. XVII, pp. 335-338 (1991).

[2] Gillespie, J., Bozada, C., Kehias, L., Quach, T., Mah, M., Worley, R., Cummins, S., and Eppers, C., High Density Test Reticle, U.S. Air Force Wright Laboratory Interim Report WL-TR-93-5011 (February 1993).

[3] Schuster, C. E., and Linholm, L. W., *Semiconductor Measurement Technology:* Test Structure Assessment Document: DC Parametric Test Structures and Test Methods for Monolithic Microwave Integrated Circuits (MMICs), NIST Special Publication (to be published).

[4] Mayo, R. N., Arnold, M. H., Scott, W. S., Stark, D., and Hamachi, G., 1990 DECWRL/Livermore Magic Release, Regents of the University of California, Lawrence Livermore National Labs, Stanford University, and Digital Equipment Corp. (September 1990).

[5] Kopanski, J. J., and Schuster, C. E., Review of Semiconductor Microelectronic Test Structures with Applications to Infrared Detector Materials and Processes, *Semicond. Sci. Technol.* **8**, 892-894 (July 1993).

[6] Suehle, J. S., Linholm, L. W., and Kafadar, K., A Method for Selecting a Minimum Test Chip Sample Size to Characterize Microelectronic Process Parameters, Proc. 1983 Custom Integrated Circuits Conf., Rochester, NY, May 23-25, 1983, pp. 308-312 (1983).

[7] Rosner, B., Percentage Points for a Generalized ESD Many-Outlier Procedure, *Technometrics* **25** (2), 165-172 (1983).

Appendix A - NISTGAAS Cell Library Contents

Appendix A - NISTGAAS Cell Library Contents

This section describes how to navigate through the CAD drawing hierarchy to a particular test structure design and how to understand the checkplots found in Appendix B. In the following text, references to process layers or constructs are made in terms of color and pattern. The colors pertain to what is seen when viewing the CIF format of NISTGAAS, while the patterns (in black and white) pertain to the Appendix B checkplots.

A.1 List of Test Structures

For each test structure type, a number of design variations related to process layers and size are included. Table A-1 shows the available design variations and associated cell names. The cell name is a concatenation of the test structure type, process layer, and size. In the cell name, the notation "{2,3,4,6,8,10,12}" indicates that seven separate cells actually exist, with the last character of their names being "2", "3", ... "12", respectively. The information in the Layout Label column relates to the library cell hierarchy as follows.

A.2 Library Hierarchy

When the NISTGAAS file is viewed, the top-level drawing, shown in figure A-1, has blocks whose labels show only partially. The numbers to the left of each set of blocks are keyed to table A-1, to indicate the content of the layout label blocks at the next lower level of the drawing hierarchy. When a block at the lower level is viewed, as shown in figure A-2, the layout label in table A-1 is clearly seen in the large full-length block on the left. Each block to the right contains one test structure design variation (i.e., one cell), whose cell name corresponds to an entry in table A-1.

A.3 Process Layer Designators

Upon viewing a cell, a checkplot of the test structure design is seen. Checkplots for each test structure type are included in the specifications in Appendix B. The meaning of the colors and patterns is defined in the top-level drawing (figure A-1), in the legend found in the lower left corner, where the process layer names are partially spelled out in their corresponding color or pattern. For convenience when viewing a design on the screen and in Appendix B, the mapping of process layer to color and pattern is shown in table A-2. As an aid in identifying the design when the fabricated test structure is viewed under a microscope or on a CAD monitor, most designs include a layer designator, formed in thick metal and placed adjacent to a run of the layer.

A.4 Cell Contents

Most cells include two independent sets of probe pads to accommodate either a horizontal-vertical or a 0°-90° combination of orientation variations. The convention used is: the upper set of pads is the horizontal or 0° orientation and the lower set of pads is the vertical or 90° orientation. Both sets of pads can be probed with one touchdown of a 2 x 6 probe card.

Table A-1. NISTGAAS Test Structures and CAD File Locations (Page 1 of 2)

TEST STRUCTURE TYPE	PROCESS LAYER COMBINATION	CAD File Location	
		Layout Label	Cell Name
Kelvin-Cross Interfacial Contact Resistor (Four-Pad → conres, Shared-Pad → conressh)	ohmic-to-mesa first metal-to-ohmic	❶ labelconres1	conres_om_{2,3,4,6,8,10,12} conres_m1o_{2,3,4,6,8,10,12} conressh_o_{2,3,4,6,8,10,12}
	resistor-to-ohmic first metal-to-resistor	❷ labelconres2	conres_ro_{2,3,4,6,8,10,12} conres_m1r_{2,3,4,6,8,10,12} conressh_r_{2,3,4,6,8,10,12}
	first metal-to-gate thick metal-to-first metal	❸ labelconres3	conres_m1g_{2,3,4,6,8,10,12} conres_tm1_{2,3,4,6,8,10,12} conressh_m1_{2,3,4,6,8,10,12}
	thick metal-to-gate thick metal-to-ohmic	❹ labelconres4	conres_tg_{2,3,4,6,8,10,12} conres_to_{2,3,4,6,8,10,12} conressh_t_{2,3,4,6,8,10,12}
	gate-to-ohmic	❾ labelmisc	conres_go_{2,3,4,6,8,10,12}
Nanometer-Resolution Electrical Alignment Structure	ohmic-to-mesa gate-to-ohmic metal1-to-ohmic	❺ labelalign1	alignh_om_4 alignh_go_4 alignh_m1o_4
	thick metal-to-ohmic ohmic-to-gate thick metal-to-gate	❻ labelalign2	alignh_to_4 alignh_og_4 alignh_tg_4
	ohmic-to-mesa gate-to-ohmic metal1-to-ohmic	❼ labelalign3	alignv_om_4 alignv_go_4 alignv_m1o_4
	thick metal-to-ohmic ohmic-to-gate thick metal-to-gate	❽ labelalign4	alignv_to_4 alignv_og_4 alignv_tg_4

Table A-1. NISTGAAS Test Structures and CAD File Locations (Page 2 of 2)

TEST STRUCTURE TYPE	PROCESS LAYER COMBINATION	CAD File Location	
		Layout Label	Cell Name
Mesa/Channel van der Pauw Sheet Resistor	ohmic, mesa, gate, and first metal	⑨ labelmisc	vpauw_m_{2,3,4,6,8,10,12}
Step Coverage/Interconnect Meander	resistor-to-ohmic first metal-to-resistor first metal-to-gate air bridge	⑨ labelmisc	meander_ro_4 meander_m1r_4 meander_m1g_4 meander_air_4
Interconnect Resistor	ohmic-to-mesa first metal-to-ohmic first metal-to-resistor	⑨ labelmisc	intres_om_4 intres_m1o_4 intres_m1r_4
Cross-Bridge Resistor	mesa ohmic resistor gate first metal thick metal	⑨ labelmisc	crossbr_m_4 crossbr_o_4 crossbr_r_4 crossbr_g_1 crossbr_m1_4 crossbr_t_4
MIMIC-Standard 200 μm FET	mesa, ohmic, gate, and dielectric	⑩ labelfet	rffeth_1x200 rffetv_1x200

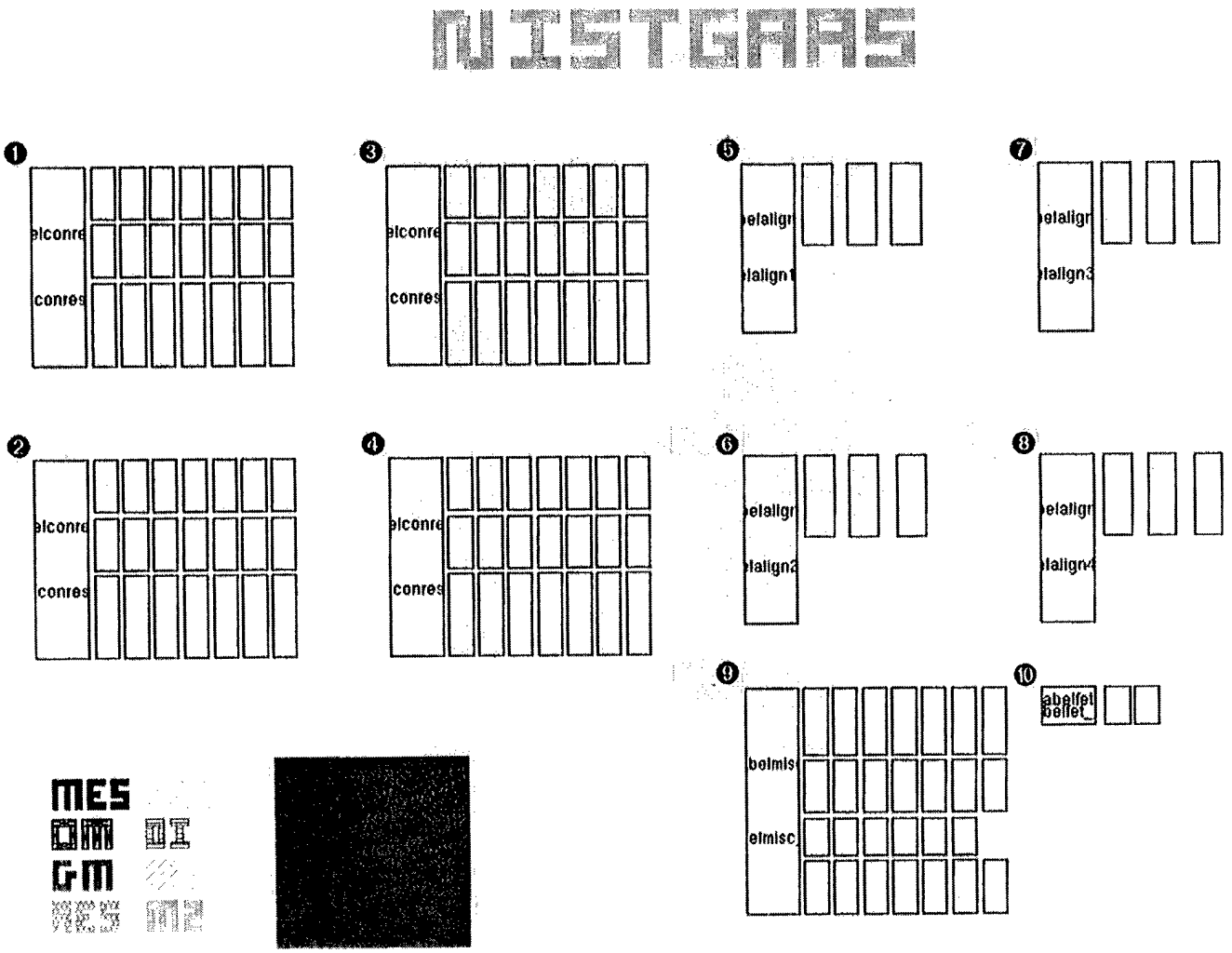


Figure A-1. NISTGAAS Top-Level CAD Drawing.

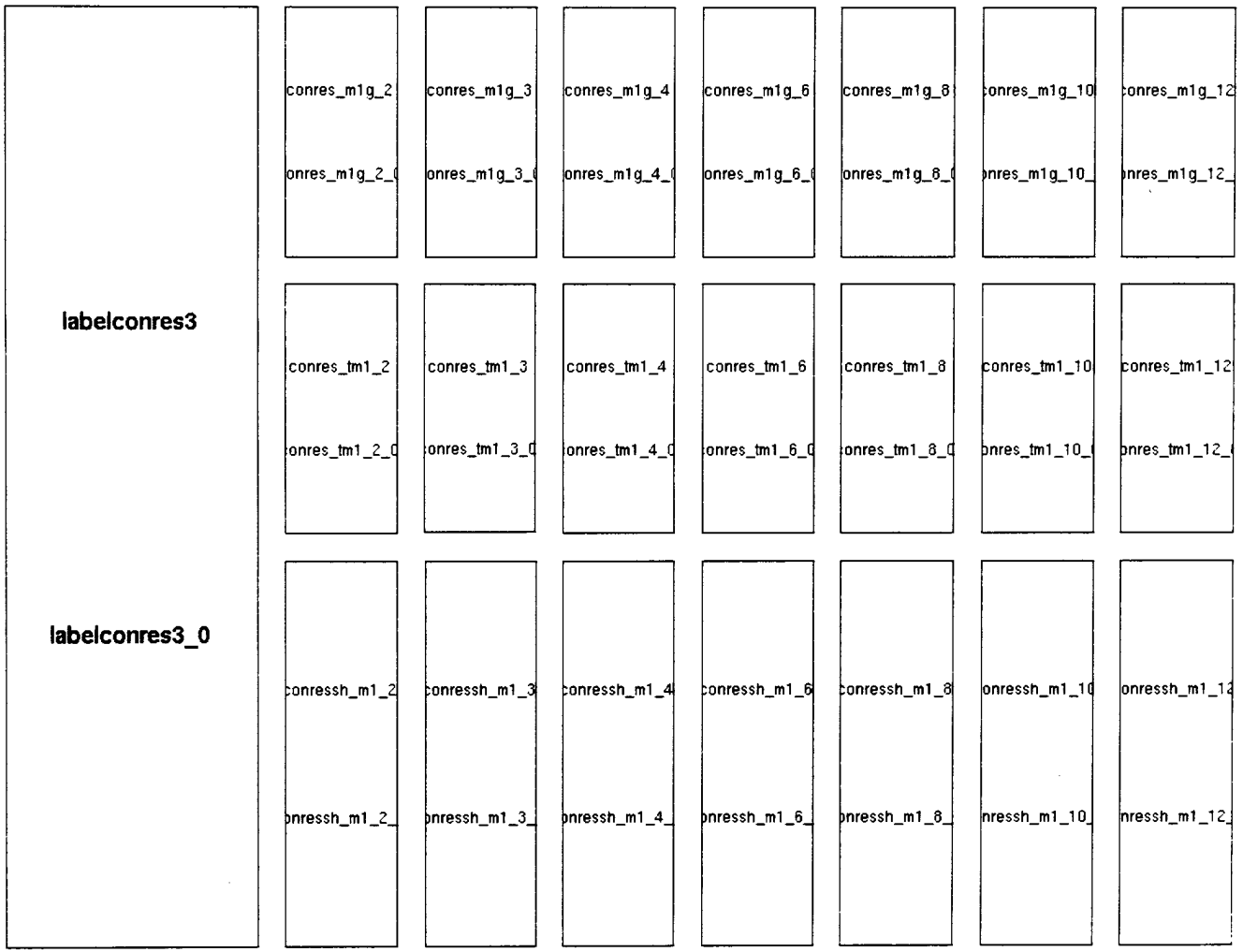


Figure A-2. NISTGAAS 2nd-Level CAD Drawing.

Table A-2. Mapping of Color/Pattern to Process Layer

PROCESS LAYER	COLOR (screen)	PATTERN (Appendix B)
mesa	green	black
ohmic	gray "x" in clear box	black "x" in clear box
resistor	brown checkerboard	gray checkerboard
gate	rust	dark gray
first metal	brown "/"	gray "/"
dielectric	gray "/" in clear box	—
air bridge	yellow "x"	—
thick metal	blue	gray

Appendix B - NISTGAAS Test Structure Specification

B.1 - Kelvin-Cross Interfacial Contact Resistor (Four-Pad)

B.2 - Kelvin-Cross Interfacial Contact Resistor (Shared-Pad)

B.3 - Nanometer-Resolution Alignment Structure

B.4 - Mesa/Channel van der Pauw Sheet Resistor

B.5 - Step Coverage/Interconnect Meander

B.6 - Interconnect Resistor

B.7 - Cross-Bridge Resistor

B.8 - MIMIC-Standard 200 μm FET

Appendix B - NISTGAAS Test Structure Specification

These notes apply to all the test structure specifications in this Appendix.

Users are responsible for selecting the exact values needed for forcing currents, tolerances, limits, or other comparative purposes cited in these procedures. Values should be process-specific and based on good engineering practice or previously demonstrated performance.

Scope

Each test structure type is specified in terms of its purpose, application, design variations, CAD checkplot, layout constraints, measurement and computation methods, analysis of results, and historical references. Some noteworthy aspects of these elements follow.

Since this document is implementation-oriented, the theoretical details of each test structure are primarily in the references. Some theoretical design considerations are reflected in the layout constraints section, although its main purpose is to help the user develop wafer-level layouts or adapt test structure designs for a different process or layer/size combination.

All design variations listed for each test structure type are available in the electronic version, as indicated in Appendix A. However, each specification includes a checkplot of only one design variation, for convenient use with this document. For a more detailed understanding of the implementation of this representative design, see the corresponding process sideview in Appendix C.

The measurement and computation methods are described independently of any particular computer-based system.

The analysis of results section is intended to help an analyst interpret what the measurements mean and how the results might be significant to process engineers and device designers.

Format

To the extent possible, the measurement procedures are described in tabular format, so they are easy to use when creating tester code. The preliminary measurement procedures, however, are in expository format to adequately explain intent, criteria for successful completion, and possible problems and solutions.

The tabular format includes columns specifying quantities to force, measure, and compute. In the **Force** and **Measure** columns, these conventions apply:

"1-3" means "current into probe pad 1 and out of probe pad 3" or "voltage at probe pad 1 with respect to probe pad 3."

"upper" and "lower" refer to the location of an interconnected set of probe pads, as cited in the layout constraints section.

Instrumentation

Some test procedures require specific, but commonly available, measurement system capabilities, as noted. Instruments with nanovolt vs microvolt resolution and teraohm vs gigaohm input impedance may be needed if the maximum current that can safely be forced will cause only a small voltage for measurement. If such instruments are not available, making such measurements is likely to produce invalid data.

All measurements should be made with dark-kits installed and microscope lights off. As MMIC measurements are affected by light, total darkness provides a reliable standard that enables meaningful comparisons of any future data from the same test structure design.

Validation of Method

Most measurement methods include a preliminary procedure to be run at "five sites" (see next paragraph) prior to the procedure intended for full-data collection. Preliminary procedures are often needed to assure that a valid measurement can be made or to determine a value to be used in the full-data procedure.

In this Appendix, references to "five sites" indicate something less than a full-data set. The exact number of sites and their location depend on the factors discussed in section 2.2. If the test structures are distributed over a whole wafer, "five sites" means "a minimum of one site near the center of the wafer and one site near the center of each quadrant, with any additional sites distributed as uniformly as possible over the rest of the wafer." If test structures are distributed some other way, use a minimum of five sites that are as evenly distributed as possible. If less than five sites are on the wafer, use all sites.

Most of the validation procedures refer to "normalized current density," which is the product of current density and layer thickness. The normalized values cited are based on a typical current density for metals of 10^6 A/cm^2 (10 mA/μm^2) and the layer thicknesses for the representative fabrication process described in section 3.2. Users should follow the methodology of the examples provided, substituting their layer characteristics to find appropriate forcing currents.

Validation of Data

Sometimes the **Compute** column computation does not reflect the most efficient computer code implementation. However, it does provide intermediate values needed to fully understand the data collected, as explained in the analysis of results section. Such analyses can be valuable in resolving problems in tester code, equipment set-up, or on the fabricated sample.

After all data are collected for all the test structure types, retest the "five sites" on the wafer to provide an assessment of the ability to consistently measure each test structure. Compare each retest data value to the full-data value for the corresponding site. If the values are not within the predetermined limits established by the user, the cause needs to be determined before meaningful analysis can be performed on the full-data set.

Before analyzing or comparing any data collected, remove outliers (that will skew the results of such investigations) by applying a robust outlier exclusion method [7].

B.1 Kelvin-Cross Interfacial Contact Resistor (Four-Pad)

PURPOSE

To determine the interfacial contact resistance and the uniformity of the interfacial contact layer.

APPLICATION

To assess the quality of a contact type.

The interfacial contact resistance is a more suitable quantity for assessing contact quality than those provided by other frequently used "contact resistance" methods. Other methods, such as the transmission line model (TLM), measure end contact resistance or indirectly measure front contact resistance. The Kelvin-cross is more accurate than these because: its Kelvin measurement eliminates parasitic resistances from each probe-to-probe pad, tap, and contact layer; its layout considerations minimize other parasitic resistances; and it is a direct measurement rather than an extrapolated value with an inherently large error.

The uniformity of the interfacial contact resistance over a range of contact sizes has been shown to be a good indicator of the quality of contacts, and hence, the performance and reliability of subsequently fabricated circuits. This uniformity is assumed, rather than measured, in the TLM method, making it unreliable for predicting contact resistance for contact sizes not measured. Such characterization can be accomplished accurately with the Kelvin-cross once it has been used to demonstrate the uniformity of the interfacial layer.

DESIGN VARIATIONS

See cell names (for contact type):

CONRES_OM_L	(ohmic-to-mesa)
CONRES_GO_L	(gate-to-ohmic)
CONRES_RO_L	(resistor-to-ohmic)
CONRES_M1O_L	(metal 1-to-ohmic)
CONRES_M1R_L	(metal 1-to-resistor)
CONRES_M1G_L	(metal 1-to-gate)
CONRES_TO_L	(thick metal-to-ohmic)
CONRES_TG_L	(thick metal-to-gate)
CONRES_TM1_L	(thick metal-to-metal 1)

where L = {2, 3, 4, 6, 8, 10, 12} indicates the design linewidth in μm.

LAYOUT CONSTRAINTS

These constraints apply to the design shown in figure B-1.

1) Each cell includes two sets of 2 x 2 probe pads, with a Kelvin-cross between each set. Each Kelvin-cross contains one contact composed of the same two layers. The upper set of pads contains the 0° orientation and the lower the 90° orientation, which has its current and voltage taps rotated counterclockwise from those in the upper set. (Measuring two such orientations enables the analysis of orientation effects; it also has long use as a measurement technique to eliminate the effects of any offsets in the measurement system.)

2) Each contact is square, is of minimum-design width, and has taps the same width as the contact edge (to eliminate parasitic resistances due to current crowding as current passes from the taps to the contact).

3) If a contact uniformity assessment is not needed, include only the minimum-design width test structure for the contact types of interest. However, if a small current will not produce a sufficient voltage (see the "Note:" in the measurement validation procedure), several larger size designs should be used to demonstrate uniformity, in order to enable extrapolation of the contact resistance for the (smaller) size of interest.

4) If determining the uniformity of a contact type, include the minimum-design width test structure and those with different size square contacts (to the extent that sufficient voltage is not a problem), and place them adjacent to each other on the wafer. At least three different sizes are needed, but five (or more) provide a better basis for the curve fit used in analyzing the data.

METHOD

For some layer combinations, the largest current that can be forced safely produces a small voltage that is measured accurately only if using a voltmeter with nanovolt resolution and teraohm input impedance.

For each design variation, perform the validation procedure in 1) below and then use the measurement procedure in 2) below to collect the intended test structure data. The validation procedure determines the forcing current to be used in the measurement procedure and assures that a valid test structure measurement can be made.

1) Determine the appropriate forcing current, I_f, needed to measure the interfacial contact resistance, R_i. This procedure requires considering the current densities of the process layers and the resolution of the voltmeter, making some preliminary measurements, and assuring that certain conditions are met. If such a determination has never been made, or the fabrication process has changed since the previous determination, then perform the following procedure; otherwise, proceed to the measurement procedure in 2).

conres_m1r_10

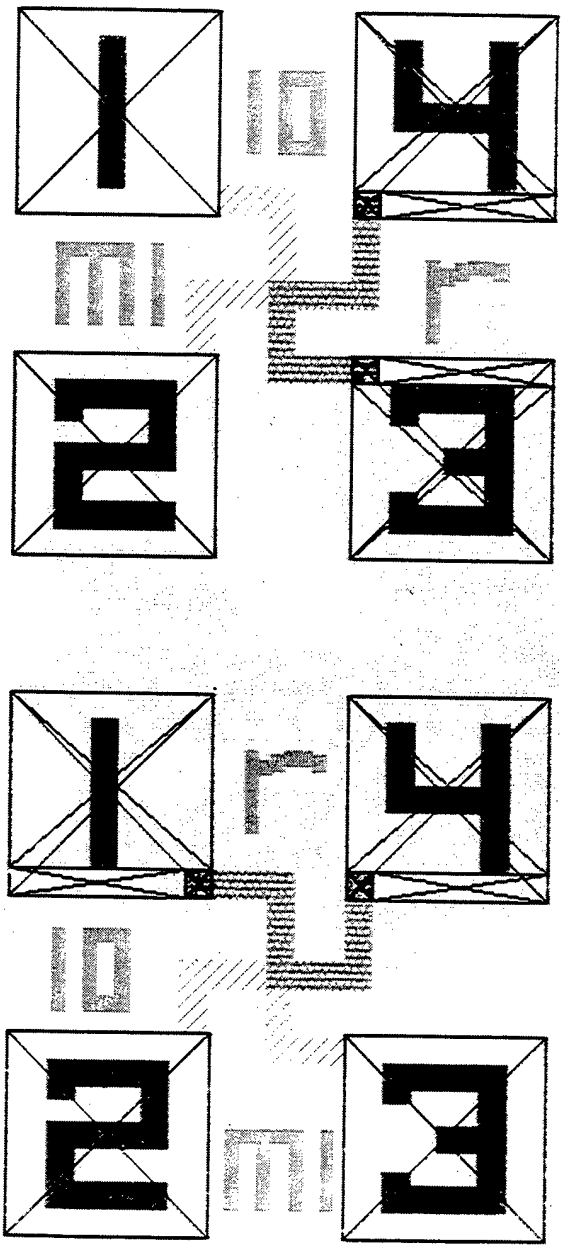


Figure B-1. Kelvin-Cross Interfacial Contact Resistor (Four-Pad).

a. Determine the (theoretical) maximum I_f that can be applied without Joule heating by identifying the lesser of the maximum normalized currents that can be sustained by the layers of the given design variation. For example, in a gate-to-ohmic contact, the maximum normalized current is limited by the ohmic layer if it is 3 mA/μm for ohmic metal and 9 mA/μm for gate metal. For a 4 μm contact edge, this means an I_f = 6 mA gives an effective normalized current of 1.5 mA/μm, or 50 % of the 3 mA/μm constraint, while an I_f = 12 mA gives 100 %.

To assure that Joule heating is avoided, limit an initial test value for I_f to a value significantly less than the constraint. Also consider any process history and knowledge about the minimum measurable and maximum sustainable currents for the particular layer types. An automated sequence of sweeps (e.g., from 50 % to 80 % of the constraint value) may be helpful in determining the I_f that best satisfies the criteria below, as several tests may be needed to assure these conditions exist.

Note: the I_f must also create a sufficient voltage across the contact for an accurate voltage measurement. The minimum voltage needed is in the decade that is 100 times the resolution of the meter. If a differential voltmeter with a resolution of 40 μV is used, the minimum voltage needed is 1 mV. If the target value for R_i for a gate-to-ohmic contact is 0.01 Ω, the minimum I_f that can be used, $I_{fmin} \geq \frac{V_{min}}{R_i}$, is 100 mA. This creates a normalized current of 25 mA/μm, which exceeds the 3 mA/μm constraint. However, if a voltmeter with a resolution of 10 nV is used, a smaller minimum voltage of 1 μV is needed; the safe I_f = 6 mA cited above creates 60 μV across the contact, which can be accurately measured with this voltmeter.

In small contacts with a small R_i and a low normalized current limit, such measurements can be difficult. If using the maximum safe current and the best resolution meter available, and the voltage is still insufficient, use a larger contact to enable forcing a larger current. Then, demonstrate uniformity for the contact type, and use the extrapolation technique suggested in layout constraints 3 and 4 to find the R_i for the smaller contact. Alternatively, the best measurement possible may be one that only indicates a low level of noise or shows that R_i is less than 1 Ω.

b. Collect and evaluate data from both orientations of the test structure. For each orientation, collect data from at least five sites that are uniformly distributed on the wafer.

For each site, sweep and plot the I-V curve from $-I_f$ to $+I_f$. To perform a sweep, force the current from pad 1 to pad 3, and measure the voltage at pad 2 with respect to pad 4 on each orientation of the test structure. In the plots for each orientation, observe whether linear operation exists and the curves are approximately centered near 0 V.

If the curves are linear and approximately centered, proceed to 2) and use the I_f just evaluated to perform the measurement procedure for the same design layer and size variation. A separate validation for other design sizes of a given layer combination is usually not necessary, as the I_f should scale linearly.

If the curves are not linear and approximately centered, the cause needs to be determined and resolved before proceeding to 2). Some potential causes may be light or heat from the measurement process, offsets in the measurement system, or problems in the fabrication process. Also, determine if both orientations and all sites provide approximately equivalent results. If not, the cause may need to be resolved before proceeding to 2). Some problems may be resolved by performing additional sweeps at progressively higher, but constrained, currents.

2) Determine the interfacial contact resistance, R_i, for a contact type:

Force	Measure	Compute
1-3, upper: $+I_f$	2-4, upper: V_{11}	
1-3, upper: $-I_f$	2-4, upper: V_{12}	$R_1 = \frac{\lvert V_{11}\rvert + \lvert V_{12}\rvert}{2\lvert I_f\rvert}$
1-3, lower: $+I_f$	2-4, lower: V_{21}	
1-3, lower: $-I_f$	2-4, lower: V_{22}	$R_2 = \frac{\lvert V_{21}\rvert + \lvert V_{22}\rvert}{2\lvert I_f\rvert}$
		$R_i = \frac{R_1 + R_2}{2}$

3) Determine the uniformity of the interfacial layer for a contact type by making the measurements in 2) above on at least three, but preferably five or more, different size contacts of that type.

ANALYSIS OF RESULTS

1) For each site, validate the data as follows. Compare the pairs of V values for a given orientation of a given contact type: V_{11} and V_{12} (0° orientation); and V_{21} and V_{22} (90° orientation). If both magnitudes in a pair are not approximately equal, the cause should be determined. Also, V_{11} and V_{21} should be positive, and V_{12} and V_{22} should be negative. Compare the R_1 and R_2 values. If they are not approximately equal, this indicates possible orientation effects. Such possibilities should be investigated by analyzing equivalent-orientation data from other test structures and devices on the wafer.

2) For the valid data for each design variation, find the mean of R_i and compare it to the target value. An important point to remember is: determining and comparing R_i values to more than two or three

significant digits should not be as important as simply determining that the measured R_i is small, where small is considered to be something less than 1 Ω.

3) To demonstrate the uniformity of the interfacial layer for a given contact type, plot the log of the mean of R_i vs the log of its associated area, A, and perform a linear curve fit. The better the points fit a straight line, the better the uniformity of the interfacial layer and the better the quality of that contact type.

REFERENCES

1) Proctor, S. J., and Linholm, L. W., A Direct Measurement of Interfacial Contact Resistance, *IEEE Electron Device Letters* **EDL-3**, 294-296 (1982).

2) Proctor, S. J., Linholm, L. W., and Mazer, J. A., Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity, *IEEE Trans. Electron Devices* **ED-30** (11), 1535-1542 (1983).

B.2 Kelvin-Cross Interfacial Contact Resistor (Shared-Pad)

PURPOSE

To determine the interfacial contact resistance and the uniformity of the interfacial contact layer.

APPLICATION

To assess the quality of a contact type.

The interfacial contact resistance is a more suitable quantity for assessing contact quality than those provided by other frequently used "contact resistance" methods. Other methods, such as the transmission line model (TLM), measure end contact resistance or indirectly measure front contact resistance. The Kelvin-cross is more accurate than these because: its Kelvin measurement eliminates parasitic resistances from each probe-to-probe pad, tap, and contact layer; its layout considerations minimize other parasitic resistances; and it is a direct measurement rather than an extrapolated value with an inherently large error.

The uniformity of the interfacial contact resistance over a range of contact sizes has been shown to be a good indicator of the quality of contacts, and hence, the performance and reliability of subsequently fabricated circuits. This uniformity is assumed, rather than measured, in the TLM method, making it unreliable for predicting contact resistance for contact sizes not measured. Such characterization can be accomplished accurately with the Kelvin-cross once it has been used to demonstrate the uniformity of the interfacial layer.

This shared-pad implementation is a space-saving alternative to the classic four-pad Kelvin-cross contact resistor, requiring 12 vs 16 pads to implement the test structure for two different contact types.

DESIGN VARIATIONS

See cell names (for contact type):

CONRESSH_O_L	(ohmic-to-mesa and metal 1-to-ohmic)
CONRESSH_R_L	(resistor-to-ohmic and metal 1-to-resistor)
CONRESSH_M1_L	(metal 1-to-gate and thick metal-to-metal 1)
CONRESSH_T_L	(thick metal-to-ohmic and thick metal-to-gate)

where L = {2, 3, 4, 6, 8, 10, 12} indicates the design linewidth in μm.

LAYOUT CONSTRAINTS

These constraints apply to the design shown in figure B-2.

1) Each cell includes a set of 2 x 6 probe pads and a total of four Kelvin-crosses, providing 0° and 90° orientations for two different contact types.

conressh_o_10

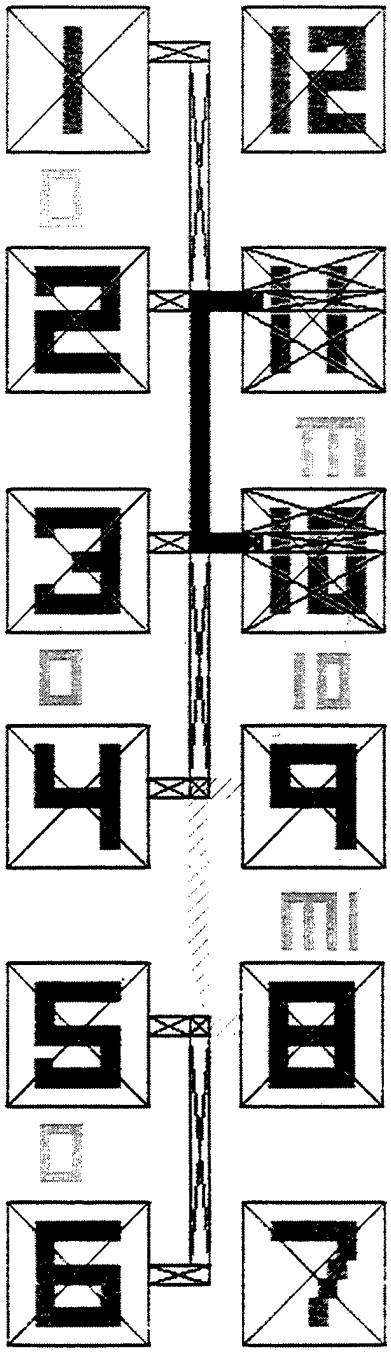


Figure B-2. Kelvin-Cross Interfacial Contact Resistor (Shared-Pad).

2) The upper two crosses implement contact type a: the top cross (at pads 2 to 11) represents the 0° orientation; the bottom cross (at pads 3 to 10) represents the 90° orientation, which has its current and voltage taps rotated counterclockwise from those in the top cross. (Measuring two such orientations enables the analysis of orientation effects; it also has long use as a measurement technique to eliminate the effects of any offsets in the measurement system.)

3) The lower two crosses, implementing contact type b, contain one of the process layers used in the upper two crosses: the layer between pads 1 and 2 is also used from pads 3 to 4 and pads 5 to 6. The top cross (at pads 4 to 9) represents the 0° orientation, and the bottom cross (at pads 5 to 8) represents the 90° orientation.

4) The NISTGAAS convention is to use the layer "shared" by the upper and lower sets of crosses as the layer name field in the test structure name.

5) Each contact is square, is of minimum-design width, and has taps the same width as the contact edge (to eliminate parasitic resistances due to current crowding as current passes from the taps to the contact).

6) If a contact uniformity assessment is not needed, include only the minimum-design width test structure for the contact types of interest. However, if a small current will not produce a sufficient voltage (see the "Note:" in the measurement validation procedure), several larger size designs should be used to demonstrate uniformity, in order to enable extrapolation of the contact resistance for the (smaller) size of interest

7) If determining the uniformity of a contact type, include the minimum-design width test structure and those with different size square contacts (to the extent that sufficient voltage is not a problem), and place them adjacent to each other on the wafer. At least three different sizes are needed, but five (or more) provide a better basis for the curve fit used in analyzing the data.

METHOD For some layer combinations, the largest current that can be forced safely produces a small voltage that is measured accurately only if using a voltmeter with nanovolt resolution and teraohm input impedance.

For each design variation, perform the validation procedure in 1) below and then use the measurement procedure in 2) below to collect the intended test structure data. The validation procedure determines the forcing current to be used in the measurement procedure and assures that a valid test structure measurement can be made.

1) Determine the appropriate forcing current, I_f, needed to measure the interfacial contact resistance, R_i. This procedure requires considering the current densities of the process layers and the resolution of the voltmeter, making some preliminary measurements, and assuring that certain conditions are met. If such a determination has never been made, or the fabrication process has changed since the previous determination, then perform the following procedure; otherwise, proceed to the measurement procedure in 2).

a. Determine the (theoretical) maximum I_f that can be applied without Joule heating by identifying the lesser of the maximum normalized currents that can be sustained by the layers of the given design variation. For example, in a gate-to-ohmic contact, the maximum normalized current is limited by the ohmic layer if it is 3 mA/μm for ohmic metal and 9 mA/μm for gate metal. For a 4 μm contact edge, this means an I_f = 6 mA gives an effective normalized current of 1.5 mA/μm, or 50 % of the 3 mA/μm constraint, while an I_f = 12 mA gives 100 %.

To assure that Joule heating is avoided, limit an initial test value for I_f to a value significantly less than the constraint. Also consider any process history and knowledge about the minimum measurable and maximum sustainable currents for the particular layer types. An automated sequence of sweeps (e.g., from 50 % to 80 % of the constraint value) may be helpful in determining the I_f that best satisfies the criteria below, as several tests may be needed to assure these conditions exist.

Note: the I_f must also create a sufficient voltage across the contact for an accurate voltage measurement. The minimum voltage needed is in the decade that is 100 times the resolution of the meter. If a differential voltmeter with a resolution of 40 μV is used, the minimum voltage needed is 1 mV. If the target value for R_i for a gate-to-ohmic contact is 0.01 Ω, the minimum I_f that can be used, $I_{fmin} \geq \frac{V_{min}}{R_i}$, is 100 mA. This creates a normalized current of 25 mA/μm, which exceeds the 3 mA/μm constraint. However, if a voltmeter with a resolution of 10 nV is used, a smaller minimum voltage of 1 μV is needed; the safe I_f = 6 mA cited above creates 60 μV across the contact, which can be accurately measured with this voltmeter.

In small contacts with a small R_i and a low normalized current limit, such measurements can be difficult. If using the maximum safe current and the best resolution meter available, and the voltage is still insufficient, use a larger contact to enable forcing a larger current. Then, demonstrate uniformity for the contact type, and use the extrapolation technique suggested in layout constraints 3 and 4 to find the R_i for the smaller contact. Alternatively, the best measurement possible may be one that only indicates a low level of noise or shows that R_i is less than 1 Ω.

b. Collect and evaluate data from both orientations and contact types of the test structure. For each orientation and contact type, collect data from at least five sites that are uniformly distributed on the wafer.

For each site, sweep and plot the I-V curve from $-I_f$ to $+I_f$. To perform a sweep for contact type a, force the current from pad 1 to pad 3 on the 0° orientation (pads 2 and 4 on the 90° orientation), and measure the voltage at pad 2 with respect to pad 11 on the 0° orientation (pads 3 and 10 on the 90° orientation). For contact type b, force the current from pad 3 to pad 5 on the 0° orientation (pads 4 and 6 on the 90° orientation), and measure the voltage at pad 4 with respect to pad 9 on the 0° orientation (pads 5 and 8 on the 90° orientation). In the plots for each orientation for a given contact type, observe whether linear operation exists and the curves are approximately centered near 0 V.

If the curves are linear and approximately centered, proceed to 2) and use the I_f just evaluated to perform the measurement procedure for the same design layer and size variation. A separate validation for other design sizes of a given layer combination is usually not necessary, as the I_f should scale linearly.

If the curves are not linear and approximately centered, the cause needs to be determined and resolved before proceeding to 2). Some potential causes may be light or heat from the measurement process, offsets in the measurement system, or problems in the fabrication process. Also, determine if both orientations and all sites provide approximately equivalent results. If not, the cause may need to be resolved before proceeding to 2). Some problems may be resolved by performing additional sweeps at progressively higher, but constrained, currents.

2) Determine the interfacial contact resistance, R_i, for two contact types: type a at pads 2, 3, 10, and 11 and type b at pads 4, 5, 8, and 9:

Force	Measure	Compute
1-3: $+I_f$	11-2: V_{a1}	
1-3: $-I_f$	11-2: V_{a2}	$R_{a1} = \frac{\lvert V_{a1}\rvert + \lvert V_{a2}\rvert}{2\lvert I_f\rvert}$
2-4: $+I_f$	10-3: V_{a3}	
2-4: $-I_f$	10-3: V_{a4}	$R_{a2} = \frac{\lvert V_{a3}\rvert + \lvert V_{a4}\rvert}{2\lvert I_f\rvert}$
3-5: $+I_f$	9-4: V_{b1}	
3-5: $-I_f$	9-4: V_{b2}	$R_{b1} = \frac{\lvert V_{b1}\rvert + \lvert V_{b2}\rvert}{2\lvert I_f\rvert}$
4-6: $+I_f$	8-5: V_{b3}	
4-6: $-I_f$	8-5: V_{b4}	$R_{b2} = \frac{\lvert V_{b3}\rvert + \lvert V_{b4}\rvert}{2\lvert I_f\rvert}$
		$R_{i(a)} = \frac{R_{a1} + R_{a2}}{2}$ $R_{i(b)} = \frac{R_{b1} + R_{b2}}{2}$

3) Determine the uniformity of the interfacial layer for a contact type by making the measurements in 2) above on at least three, but preferably five or more, different size contacts of the same type.

ANALYSIS OF RESULTS

1) For each site, validate the data as follows. Compare the pairs of V values for a given orientation of a given contact type: V_{a1} and V_{a2} (0°, type a); V_{a3} and V_{a4} (90°, type a); V_{b1} and V_{b2} (0°, type b); and V_{b3} and V_{b4} (90°, type b). If both magnitudes in a pair are not approximately equal, the cause should be determined. Also, the V_{x1} and V_{x3} values should be positive, and the V_{x2} and V_{x4} values should be negative. Compare the pairs of R values from the 0° and 90° orientations for the given contact type: R_{a1} and R_{a2} (type a); and R_{b1} and R_{b2} (type b). If both magnitudes in each pair are not approximately equal, this indicates possible orientation effects. Such possibilities should be investigated by analyzing equivalent-orientation data from other test structures and devices on the wafer.

2) For the valid data for each design variation and contact type, find the mean of R_i and compare it to the target value. An important point to remember is: determining and comparing R_i values to more than two or

three significant digits should not be as important as simply determining that R_i is small, where small is considered to be something less than 1 Ω.

3) To demonstrate the uniformity of the interfacial layer for a given contact type, plot the log of the mean of R_i vs the log of its associated area, A, and perform a linear curve fit. The better the points fit a straight line, the better the uniformity of the interfacial layer and the better the quality of that contact type.

REFERENCES

1) Proctor, S. J., and Linholm, L. W., A Direct Measurement of Interfacial Contact Resistance, *IEEE Electron Device Letters* **EDL-3**, 294-296 (1982).

2) Proctor, S. J., Linholm, L. W., and Mazer, J. A., Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity, *IEEE Trans. Electron Devices* **ED-30** (11), 1535-1542 (1983).

B.3 Nanometer-Resolution Electrical Alignment Structure

PURPOSE

To determine placement of a feature relative to two reference features.

APPLICATION

To determine the misregistration between two mask layers, in order to assess the performance of the lithography alignment process and tools.

This design enables measurements with a total uncertainty of 10 nm or less and repeatability within 1.5 nm (6 sigma), when compared to NIST length standards which are based on an optical interferometer.

Measurement results from this design are more accurate than those from the late 1970s "NBS Alignment Structure," which has 0.1 μm resolution. This design is more sensitive to slight misalignments and less sensitive to sheet resistance variations. This improvement is achieved by shortening the potentiometer bridge (to minimize material- and process-induced errors), and then compensating for the resultant systematic error of each voltage tap (due to a tap no longer being equivalent to a point contact to the bridge), which effectively shortens the length of the bridge.

Other applications are possible with this test structure. By implementing the design in a single mask layer, it can be used to evaluate the precision and accuracy of primary pattern generation or printing tools. Then, the measurements determine the placement of a feature obtained by single exposure or the registration of the printed features.

DESIGN VARIATIONS

See cell names (for mask layer types):

ALIGNH_OM_4 and ALIGNV_OM_4	(ohmic-to-mesa)
ALIGNH_GO_4 and ALIGNV_GO_4	(gate-to-ohmic)
ALIGNH_M1O_4 and ALIGNV_M1O_4	(metal 1-to-ohmic)
ALIGNH_TO_4 and ALIGNV_TO_4	(thick metal-to-ohmic)
ALIGNH_TG_4 and ALIGNV_TG_4	(thick metal-to-gate)
ALIGNH_OG_4 and ALIGNV_OG_4	(ohmic-to-gate)

The "H" or "V" following "ALIGN" denotes the different designs used to measure horizontal and vertical misregistrations. The two orientations are functionally equivalent but have different topologies which require different probing procedures. Functionally, the pads of the two orientations map as shown:

horizontal	1	2	3	4	5	6	7	8	9	10	11	12
vertical	11	1	2	6	3	12	9	10	7	4	5	8

LAYOUT CONSTRAINTS

These constraints apply to the designs shown in figures B-3 and B-4.

1) Each cell includes a set of 2 x 6 probe pads and a potentiometer-type test structure. The voltage taps at horizontal pads 5, 6, 7, 8, and 11 (vertical pads 3, 12, 9, 10, and 5) are used to determine the length-shortening effects and to assess line uniformity.

2) The other voltage taps implement three fixed offsets. The first offset is used to determine the misregistration and the other two provide known values which are used for measurement verification. Three taps define each offset, which is the distance from the center of the "middle" tap with respect to the center between the centers of the "end" taps. The first offset is 0 μm (horizontal pads 2, 4, and 9; vertical pads 1, 6, and 7). The other offsets are +1 μm (horizontal pads 5, 3, and 2; vertical pads 3, 2, and 1) and –1 μm (horizontal pads 9, 10, and 11; vertical pads 7, 4, and 5).

3) The spacings of the voltage taps relate to the design length of a bridge segment, *L*, whose length is 20 μm. The following spacings cannot be changed without making other design considerations and changing the documented methods for verification and measurement.

between centers of taps from		
horizontal pads	vertical pads	spacing (μm)
5 to 2	3 to 1	
2 to 9	1 to 7	
9 to 11	7 to 5	
11 to 8	5 to 10	L
6 to 5	12 to 3	
8 to 7	10 to 9	$3L$
2 to 4	1 to 6	
4 to 9	6 to 7	$L/2$
5 to 3	3 to 2	
10 to 11	4 to 5	$(L/2) + 1$
3 to 2	2 to 1	
9 to 10	7 to 4	$(L/2) - 1$

4) The taps for measuring voltages (all horizontal pads except 1 and 12; all vertical pads except 11 and 8) must all cross the bridge and extend from the same side of the bridge. The extension of each tap must be ≥ 2 times the width of the tap. (These constraints minimize the effects of inside corner rounding.)

5) All taps and the bridge are implemented in the minimum-design linewidth. To evaluate the limits of the current process or to design a

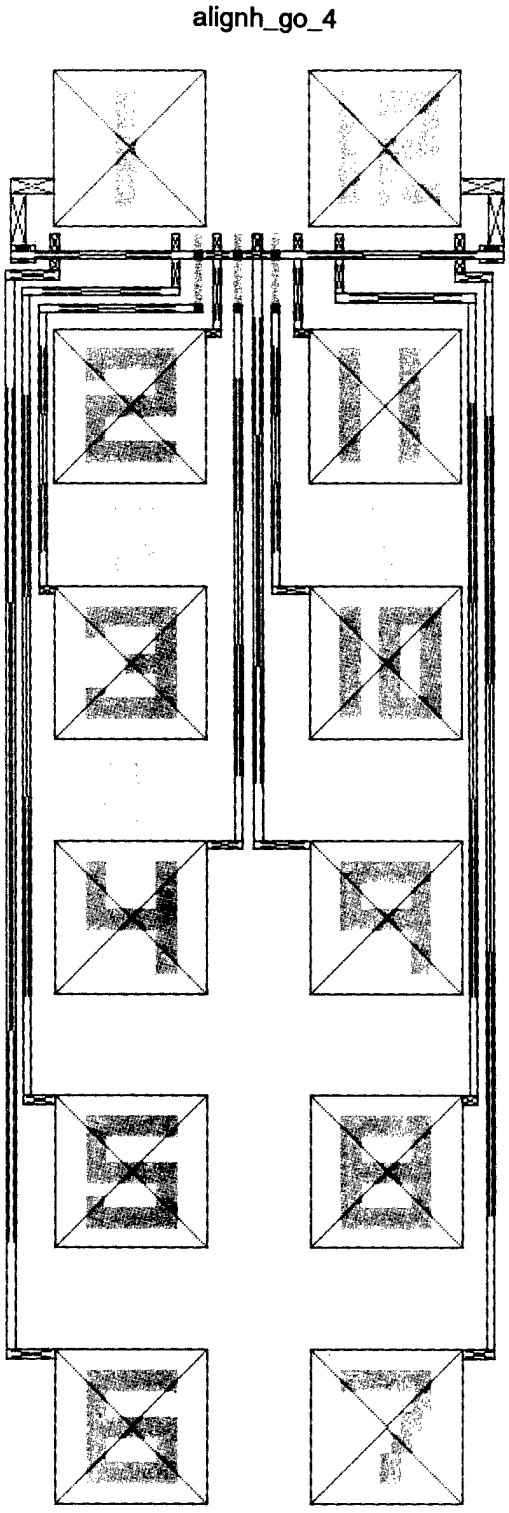


Figure B-3. Nanometer-Resolution Electrical Alignment Structure (Horizontal).

alignv_go_4

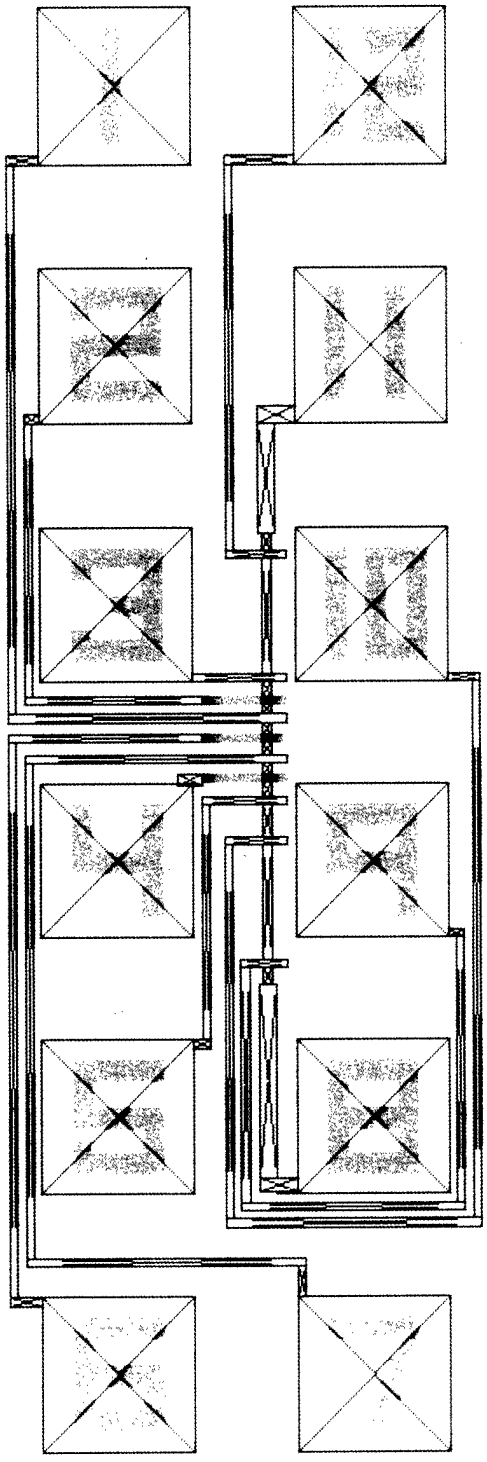


Figure B-4. Nanometer-Resolution Electrical Alignment Structure (Vertical).

mask set that is also usable on future, smaller-geometry processes, include smaller-design linewidth test structures as well. This design can be scaled down to 0.7 μm; smaller geometries cannot be reliably fabricated due to imaging nonlinearities in current lithography tools.

6) The NISTGAAS convention is to implement the bridge in the lower mask layer and the center tap of the measurement and fixed offset taps in the upper mask layer. Thus, in the gate-to-ohmic design, the bridge is ohmic metal, and the measurement and fixed offset center taps are gate metal. To minimize the effect of ohmic sheet resistance variations in some processes, this implementation can be inverted to obtain a measurement least affected by these variations: the longer length bridge uses gate metal and the shorter length taps use the more variable ohmic metal. This inverse implementation is the "OG" design, provided in addition to the conventional "GO" design.

7) A designator in thick metal is provided for easy identification when viewing these structures. For the horizontal (vertical) cells, the letter below (above) pad 2 indicates the layer of the bridge, while the letter below (above) pad 11 indicates the layer of the center taps.

8) Each cell includes metal runs that are outside the 2 x 6 probe-pad area. These runs extend from the pad 2 and pad 11 sides: by 24 μm and 22 μm, respectively, for the ALIGNH cell, and by 16 μm and 16 μm, respectively, for the ALIGNV cell. While any other NISTGAAS cell can be placed adjacent to an ALIGNH or ALIGNV cell without violating any design rule, the user needs to assure that this is also true if placing non-NISTGAAS constructs adjacent to these cells.

METHOD For each design variation, perform the validation procedure in 1) below and then use the measurement procedure in 2) below to collect the intended test structure data. The validation procedure determines the forcing current to be used in the measurement procedure and assures that a valid test structure measurement can be made.

1) Determine the appropriate forcing current, I_f, needed to determine the mask layer misregistration. This procedure requires considering the current densities of the process layers and the resolution of the voltmeter, making some preliminary measurements, and assuring that certain conditions are met. If such a determination has never been made, or the fabrication process has changed since the previous determination, then perform the following procedure; otherwise, proceed to the measurement procedure in 2).

a. Determine the (theoretical) maximum I_f that can be applied without Joule heating by identifying the lesser of the maximum normalized currents that can be sustained by the layers of the given design variation. For example, in a gate-to-ohmic design, the maximum

normalized current is limited by the ohmic layer if it is 3 mA/μm for ohmic metal and 9 mA/μm for gate metal. For a 4 μm bridge, this means an I_f = 10 mA gives an effective normalized current of 2.5 mA/μm, or 83 % of the 3 mA/μm constraint, while an I_f = 12 mA gives 100 %.

To assure that Joule heating is avoided, limit an initial test value for I_f to a value significantly less than the constraint. Also consider any process history and knowledge about the minimum measurable and maximum sustainable currents for the particular layer types. An automated sequence of sweeps (e.g., from 50 % to 80 % of the constraint value) may be helpful in determining the I_f that best satisfies the criteria below, as several tests may be needed to assure these conditions exist.

Note: the I_f must also create a sufficient voltage in the bridge, V_b, for an accurate voltage measurement. The minimum voltage needed is in the decade that is 100 times the resolution of the meter. If a differential voltmeter with a resolution of 40 μV is used, the minimum voltage needed is 1 mV. The minimum V_b to be measured will occur for the minimum bridge length of 9 μm. For a 4 μm ohmic bridge design (with target sheet resistance, R_{sh}, of 0.5 Ω), the minimum I_f that can be used, $I_{fmin} \geq \frac{V_{bmin} W}{R_{sh} L}$, is 0.89 mA. This creates a normalized current of 0.22 mA/μm, which is well below the 3 mA/μm constraint. More than a minimum I_f should be used when possible. If the sufficient and safe I_f = 10 mA cited above is used, the minimum V_b to be measured will be 11.2 mV, which can be accurately measured with this voltmeter.

b. Collect and evaluate data from both orientations of the test structure. For each orientation, collect data from at least five sites that are uniformly distributed on the wafer.

For each site, sweep and plot the I-V curve from $-I_f$ to $+I_f$. To perform a sweep, force the current from pad 1 to pad 12 on the horizontal structure (pads 11 and 8 on the vertical structure), and measure the voltage at pad 2 with respect to pad 3 on the horizontal structure (pads 1 and 2 on the vertical structure). In the plots for each orientation, observe if linear operation exists and the curves are approximately centered near 0 V.

If the curves are linear and approximately centered, proceed to 2) and use the I_f just evaluated to perform the measurement procedure for the same design layer variation.

If the curves are not linear and approximately centered, the cause needs to be determined and resolved before proceeding to 2). Some potential causes may be light or heat from the measurement process, offsets in the measurement system, or problems in the fabrication process. Also, determine if both orientations and all sites provide approximately equivalent results. If not, the cause may need to be resolved before

proceeding to 2). Some problems may be resolved by performing additional sweeps at progressively higher, but constrained, currents.

2) Determine the misregistration between two mask layers by applying the following procedure and the analysis of results procedures to both orientations of the test structure.

a. Determine and test the *a* values and *b* values as indicated in Steps 1 and 2 in the table below, to assure that the voltage taps are functional and the bridge is uniform. If these values are not within T, a predetermined tolerance (see next paragraph), the computations in Step 3 are not meaningful for this site. In this case, log all of the data values for this site as invalid and proceed to the next site. (Once data for all sites are collected, analyze the invalid data sites as indicated in the analysis of results section.) If all the voltages measured in Steps 1 and 2 are valid, continue to Step 3.

b. In Steps 1 and 2, the value of T is a function of the length and resistivity of the material, as well as an uncertainty value, k, supplied by the user. The value for k is less than the uncertainty desired for the measurement of misregistration. The value for T is then determined by $T = \frac{k}{L} \cdot (V_4 + V_5)$. The V_4 and V_5 values are found as indicated in Step 1 in the table. Thus, if the desired measurement uncertainty is 20 nm, and the $V_4 + V_5$ sum is 2 mV, the value for T is 2 μV.

c. In Step 3, average the Vs measured in Steps 1 and 2, as shown in the table. Use the indicated averages to find the length-shortening of the bridge due to the voltage taps: δL_L for one tap in the lower metal layer, and δL_U for one tap in the upper metal layer. Use the δLs and Vs indicated to determine x_p and x_m, verification measurements of the fixed offsets of +1 μm and –1 μm, and to determine x, the measured value of the mask misregistration at the site.

See next page for table.

Force			Measure			Compute (and test tolerances)
H	V		H	V		
1-12	11-8	$+I_f$	6-5 5-3 3-2 2-4 4-9 9-10 10-11 11-8 8-7 5-11 6-7	12-3 3-2 2-1 1-6 6-7 7-4 4-5 5-10 10-9 3-5 12-9	V_{1a} V_{2a} V_{3a} V_{4a} V_{5a} V_{6a} V_{7a} V_{8a} V_{9a} V_{10a} V_{11a}	Step 1 $a_1 = V_{10a} - (V_{2a} + V_{3a} + V_{4a} + V_{5a} + V_{6a} + V_{7a})$ $a_2 = V_{11a} - (V_{1a} + V_{10a} + V_{8a} + V_{9a})$ $a_3 = V_{1a} - V_{9a}$ if $\{(a_1 \rangle T) \cup (a_2 \rangle T) \cup (a_3 \rangle T)\}$ then {log "invalid" x_p, x_m, and x for site; go to next site} else {continue to next Step}
1-12	11-8	$-I_f$	as in Step 1	as in Step 1	V_{1b} to V_{11b}	Step 2 repeat Step 1, substituting "b" for "a" and "b" for "a": - measure values V_{1b} to V_{11b} - compute and test values b_1 to b_3
						Step 3 $V_n = \frac{V_{na} + V_{nb}}{2}$, where n = {1, 2, ... 10} $V_c = \frac{V_1 + V_9}{2}$ $\delta L_L = \frac{V_c - 3V_8}{V_c - V_8} \cdot L$ $\delta L_U = -\frac{2L}{3} \cdot \frac{V_{10} - 3V_8}{V_c - V_8}$ $x_p = \frac{V_2 - V_3}{V_2 + V_3} \cdot \frac{L - \delta L_L - \delta L_U}{2}$ $x_m = \frac{V_6 - V_7}{V_6 + V_7} \cdot \frac{L - \delta L_L - \delta L_U}{2}$ $x = \frac{V_4 - V_5}{V_4 + V_5} \cdot \frac{L - \delta L_L - \delta L_U}{2}$

ANALYSIS OF RESULTS

1) If invalid measurements are found in Step 1, further analysis is needed to determine whether this is due to measurement system problems or processing problems. To begin such an investigation, remeasure each invalid data site to see if the problem is reproducible, assuring that good contact exists between the probes and probe pads. If valid data cannot be obtained with careful, manual measurement, log the V values and the x values (in an area separate from the database for the valid data).

Analyze the V_1 to V_{11} values to see if a particular bridge segment is a frequent problem. Check that the components of V_1, V_{10}, and V_{11} are consistent with their measured values, and check that $V_4 = V_5$, $V_2 = V_7$, and $V_3 = V_6$. If measurement system problems cannot be identified and a significant amount of data remains invalid, other process problems may exist. Analyze and correlate other test structure data to investigate this possibility.

2) Perform this analysis on the valid data collected for each orientation of the test structure. Compare the verification measurements, x_p and x_m, to their corresponding design values of +1 μm and –1 μm, as follows. Find the mean of all the valid measurements for each quantity: x_p, x_m, and x. Plot each mean value vs its corresponding design value; perform a linear curve fit for the three points. Then, subtract the value of the y-intercept from the mean of the x_p values and from the mean of the x_m values. If either result is significantly different from its corresponding design value (i.e., not within the desired range given the k value specified by the user), further evaluation is needed as described in the next two paragraphs.

If stepper-based lithography was used to implement the test structures, distinguish between a patterning error and either a measurement system error or a processing problem as follows. For each site, plot the x_p, x_m, and x values. If all the plots consistently show three points not in an acceptably straight line, then a patterning error is likely. If, in the set of plots with the three points not in an acceptably straight line, the random (non-repeated) errant points can be treated as outliers, then a measurement system or process error is likely.

If stepper-based lithography was not used, data from more than one wafer is needed to perform further analysis. If data exist for a statistically significant number of wafers, for each site on each wafer, plot the x_p, x_m, and x values. For a given site, if the plots for all the wafers show the same relationship between the three points, then a systematic error exists.

3) For each orientation, the misregistration between the two mask layers is the extracted value of the y-intercept, as determined in 2) above. A smaller value means lesser misregistration. Positive values from the horizontal (vertical) structure indicate that features fabricated on the wafer near the site are more to the right (bottom) than they would be if

they were perfectly aligned. The difference between the mean of the measured x value and the extracted misregistration value is the residual error (due mainly to imperfections in the material or patterning of the mask layer), as described in Reference 2.

4) Examine the individual and overall effects of both the horizontal and vertical misregistration by creating wafer maps of full-wafer data for x_p, x_m, and x. Translational (run-out) or rotational effects, can be extracted, as discussed in Reference 4.

REFERENCES

1) Linholm, L. W., Allen, R. A., and Cresswell, M. W., Microelectronic Test Structures for Feature Placement and Electrical Linewidth Metrology, in the *Handbook of Critical Dimension Metrology and Process Control*, Vol. CR52, K. M. Monahan, Ed. (SPIE, Bellingham, WA, 1994), pp. 91-118.

2) Allen, R. A., Cresswell, M. W., Linholm, L. W., Owen, J.C., III, Ellenwood, C.H., Hill, T. A., Benecke, J. D., Volk, S. R., and Stewart, H. D., Application of the Modified Voltage-Dividing Potentiometer to Overlay Metrology in a CMOS/Bulk Process, Proceedings of the 1994 IEEE International Conference on Microelectronic Test Structures, San Diego, CA, March 22-24, 1994, Vol. 7, pp. 51-56.

3) Cresswell, M. W., Penzes, W. B., Allen, R. A., Linholm, L. W., Ellenwood, C. H., and Teague, E. C., Electrical Test Structure for Overlay Metrology Referenced to Absolute Length Standards, Proceedings of SPIE, International Society of Optical Engineering, *Integrated Circuit Metrology, Inspection, and Process Control VIII* **2196**, 512-521 (1994).

4) Russell, T. J., Leedy, T. F., and Mattis, R. L., A Comparison of Electrical and Visual Alignment Test Structures for Evaluating Photomask Alignment in Integrated Circuit Manufacturing, Tech. Digest, Intl Electron Devices Meeting, Washington, DC, December 5-7, 1977, pp. 7A-7F (1977).

B.4 Mesa/Channel van der Pauw Sheet Resistor

PURPOSE

To determine active layer sheet resistance and channel thickness.

APPLICATION

To assess the quality of the active layer and the channel and to assess the potential performance of a FET formed using the active layer and channel.

If channel thickness for a transistor is needed as a monitor or predictor of FET performance, this test structure can replace the conventional van der Pauw test structure fabricated in the active layer and provide the measurement needed to determine channel thickness. A van der Pauw structure fabricated in the active (mesa) layer enables direct measurement of the sheet resistance of the mesa. A gated van der Pauw structure fabricated in the channel (recess) enables direct measurement of the sheet resistance of the channel, which can be used with doping profile information to determine channel thickness.

This method of determining channel thickness is inherently more accurate than methods using the transmission line model (TLM) test structure because it is more direct and accurate. The TLM-based methods require multiple measurements on each test structure and multi-step graphical and extrapolation techniques to obtain channel thickness. They also assume that the TLM can provide an accurate contact resistance value (see sections B.1 and B.2) and that a uniform contact resistance does exist over the several hundred micrometers from which TLM measurements are made.

DESIGN VARIATIONS

See cell names:

VPAUW_M_L

where $\mathbb{L} = \{2, 3, 4, 6, 8, 10, 12\}$ indicates the design linewidth in μm.

LAYOUT CONSTRAINTS

These constraints apply to the design shown in figure B-5.

1) Each cell includes two van der Pauw sheet resistors. The lower 4 pads of each cell contain the mesa sheet resistor. The upper 6 pads contain the channel sheet resistor and include a gate connection to bias the channel, as explained in the measurement method section.

2) The arms of the van der Pauw cross must have a length ≥ 2 times their width.

3) The linewidth of the test structure implemented on the wafer should be the same as the width of the recess (bottom) in the device of interest.

vpauw_m_12

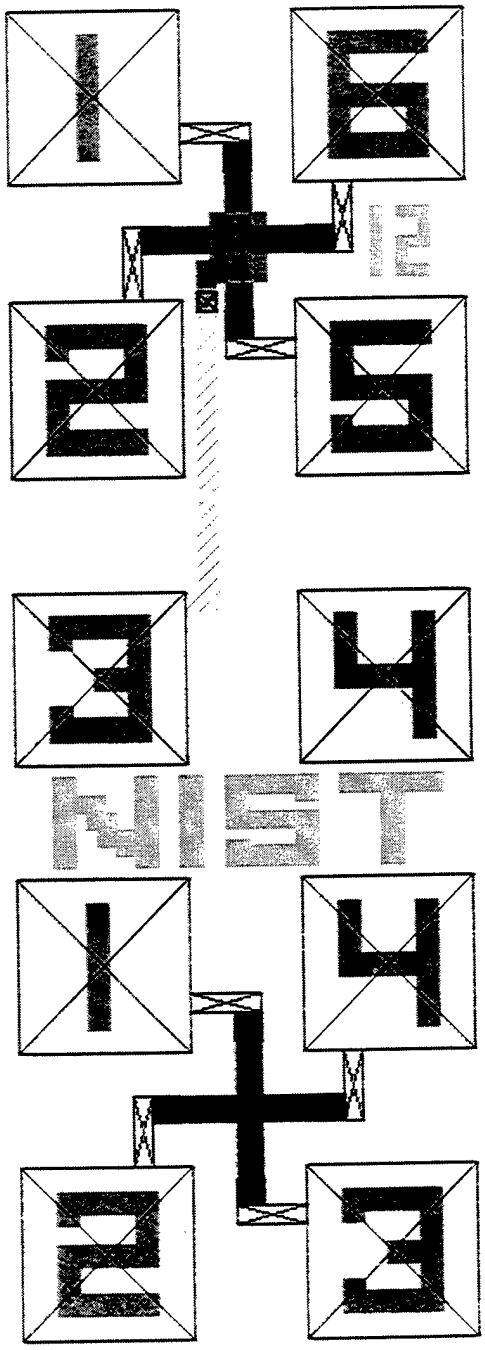


Figure B-5. Mesa/Channel van der Pauw Sheet Resistor .

METHOD 1) Perform this validation procedure and then use the measurement procedure starting at 2) below to collect full-wafer data. This validation procedure assures that a valid test structure measurement can be made.

a. Select a forcing current, I_f, based on process history or other knowledge (0.5 mA is typical for a MESFET process).

b. Collect and evaluate data from the 4-pad and 6-pad structures. For each structure, collect data from at least five sites that are uniformly distributed on the wafer.

For each site, sweep and plot the I-V curve from $-I_f$ to $+I_f$. To perform a sweep, make the conventional 0° and 90° van der Pauw measurements as follows. Force the current from pad 2 to pad 1, and measure the voltage at pad 3 with respect to pad 4; this represents the 0° measurement. For the 90° measurement, force the current from pad 3 to pad 2, and measure the voltage at pad 4 with respect to pad 1. In the plots for each measurement orientation, observe whether linear operation exists and the curves are approximately centered near 0 V.

If the curves are linear and approximately centered, proceed to 2) and use the I_f just evaluated to perform the measurement procedure for the same design size variation. A separate validation for other design sizes is usually not necessary, as the I_f should scale linearly.

If the curves are not linear and approximately centered, the cause needs to be determined and resolved before proceeding to 2). Some potential causes may be light or heat from the measurement process, offsets in the measurement system, or problems in the fabrication process. Also, determine if both orientations at a site and for all sites provide approximately equivalent results. If not, the cause may need to be resolved before proceeding to 2). Some problems may be resolved by performing additional sweeps at other currents, based on process history.

2) Determine the sheet resistance of the mesa, $R_{sh(m)}$, using the 4-pad van der Pauw cross sheet resistor (lower 4 pads):

Force	Measure	Compute
2-1: $+I_f$	3-4: V_1	
2-1: $-I_f$	3-4: V_2	$R_{m1} = \frac{\lvert V_1\rvert + \lvert V_2\rvert}{2\lvert I_f\rvert}$
3-2: $+I_f$	4-1: V_3	
3-2: $-I_f$	4-1: V_4	$R_{m2} = \frac{\lvert V_3\rvert + \lvert V_4\rvert}{2\lvert I_f\rvert}$
		$R_{sh(m)} = \frac{\pi}{\ln 2} \cdot \frac{R_{m1} + R_{m2}}{2}$

3) Determine the sheet resistance of the channel, $R_{sh(ch)}$, using the 6-pad van der Pauw cross sheet resistor (upper 6 pads):

Force	Measure	Compute
2-1: $+I_f$	5-6: V_1	
2-1: $-I_f$	5-6: V_2	$R_{ch1} = \frac{\lvert V_1\rvert + \lvert V_2\rvert}{2\lvert I_f\rvert}$
5-2: $+I_f$	6-1: V_3	
5-2: $-I_f$	6-1: V_4	$R_{ch2} = \frac{\lvert V_3\rvert + \lvert V_4\rvert}{2\lvert I_f\rvert}$
		$R_{sh(ch)} = \frac{\pi}{\ln 2} \cdot \frac{R_{ch1} + R_{ch2}}{2}$

4) To determine how a change in gate bias affects the channel sheet resistance, perform the procedure in 3) above while also forcing the desired V_g at pad 3. The resultant channel thickness and sheet resistance values can then be used as desired in conjunction with doping profile information (see analysis of results section).

ANALYSIS OF RESULTS

1) For each site, validate the data as follows. For the mesa data, compare the pairs of V values for each measurement orientation: V_1 and V_2 (0° measurement); and V_3 and V_4 (90° measurement). If the compared magnitudes are not approximately equal, the cause should be determined. Also, V_1 and V_3 should be positive, and V_2 and V_4 should be negative. Compare the R_{m1} and R_{m2} values. If they are not approximately equal, this indicates possible orientation effects. Such possibilities should

be investigated by analyzing equivalent-orientation data from other test structures and devices on the wafer. Also perform this analysis for the corresponding V and R values for the channel.

2) For the valid data, find the means of $R_{sh(m)}$ and $R_{sh(ch)}$ and compare them to the target values.

3) Using the $R_{sh(ch)}$ value, read the channel thickness from a graph of sheet resistance and thickness, derived from doping profile data obtained either from measurement or simulation.

REFERENCES

1) Buehler, M. G., and Thurber, W. R., An Experimental Study of Various Cross Sheet Resistor Test Structures, *J. Electrochem. Soc.* **125** (4), 645-650 (1978).

2) Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers, *J. Electrochem. Soc.* **125** (4), 650-654 (1978).

3) Buehler, M. G., and Thurber, W. R., Measurement of the Resistivity of a Thin Square Sample with a Square Four-Probe Array, *Solid-State Electronics* **20**, 403-406 (1977).

4) David, J. M., and Buehler, M. G., A Numerical Analysis of Various Cross Sheet Resistor Test Structures, *Solid-State Electronics* **20**, 539-543 (1977).

5) Buehler, M. G., and Thurber, W. R., A Planar Four-Probe Test Structure for Measuring Bulk Resistivity, *IEEE Trans. Electron Devices* **ED-23** (8), 968-974 (1976).

6) Williams, R., *Modern GaAs Processing Methods* (Artech House, Norwood, MA, 1990), p. 303.

B.5 Step Coverage/Interconnect Meander

PURPOSE

To detect step coverage problems between two conducting layers.

APPLICATION

To assess qualitatively if catastrophic step coverage problems exist.

Step coverage is most often a problem in a planar process when the thickness of the upper layer is not more than several times as thick as the lower layer. If step coverage problems exist, they are most frequently catastrophic and therefore yield-limiting. Such problems are observable as loss of continuity in a series chain of contacts.

This design is intended to detect, but not locate or rigorously quantify, catastrophic step coverage failures. For this application, a large number of contacts are not needed for robust statistics or detectability, so the design is compact and probe-pad compatible with the rest of the cell library. Because this design has a small number of contacts, it should not be used to determine a failure rate, as some similar but larger designs could be used.

DESIGN VARIATIONS

See cell names (for mask layer types):

MEANDER_RO_4	(resistor-to-ohmic)
MEANDER_M1R_4	(metal 1-to-resistor)
MEANDER_M1G_4	(metal 1-to-gate)
MEANDER_AIR_4	(air bridge)

LAYOUT CONSTRAINTS

These constraints apply to the design shown in figure B-6.

1) Each cell includes two sets of 2 x 2 probe pads, with a meander between each set. Each meander contains 170 contacts, all composed of the same layers, with taps after the 4th and 12th contacts. The upper set of pads contains horizontal contacts and the lower vertical contacts, with the current and voltage taps rotated counterclockwise from those in the upper set. (Measuring two such orientations enables the analysis of orientation effects; it also has long use as a measurement technique to eliminate the effects of any offsets in the measurement system.)

2) Each contact is square, is of minimum-design width, and has taps the same width as the contact edge (to eliminate parasitic resistances due to current crowding as current passes from the taps to the contact). The adjacent contacts are separated by the minimum-design spacing. Only minimum-design widths and spacings are implemented.

meander_m1g_4

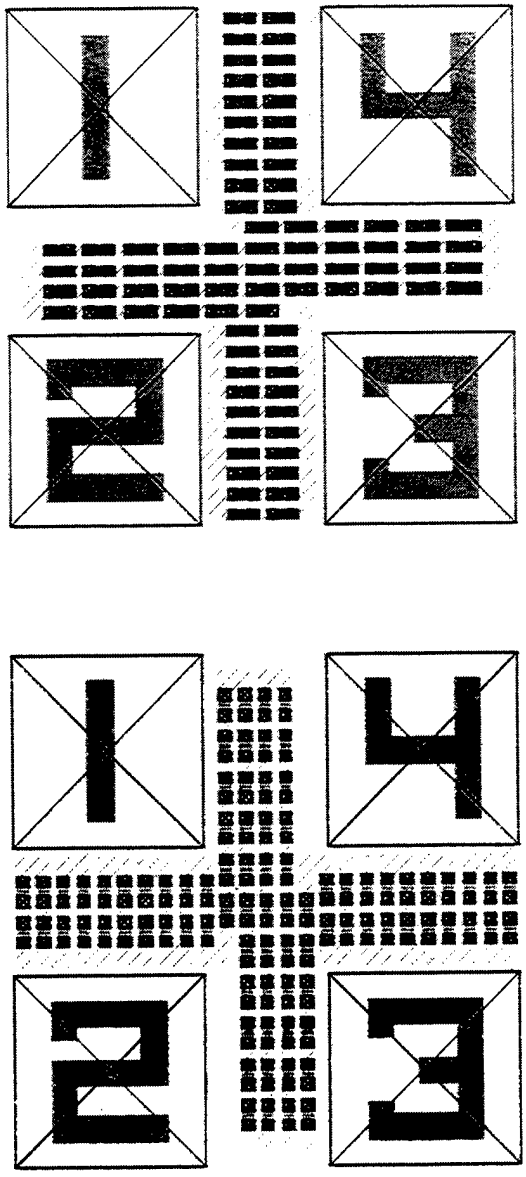


Figure B-6. Step Coverage/Interconnect Meander.

METHOD

1) Determine if an open circuit exists for a contact type by measuring continuity for different length contact chains. Select the forcing current, I_f, based on process history or other knowledge (1 mA is typical for a MESFET process).

Force	Measure
1-3, upper: I_f	1-3, upper: V_{11}
2-3, upper: I_f	2-3, upper: V_{12}
1-4, upper: I_f	1-4, upper: V_{13}
4-2, lower: I_f	4-2, lower: V_{21}
1-2, lower: I_f	1-2, lower: V_{22}
4-3, lower: I_f	4-3, lower: V_{23}

ANALYSIS OF RESULTS

1) If the voltmeter does not indicate a compliance limit on V_{11} or V_{21} for a given step type, then step coverage should not be a problem. Otherwise, apply 2) below to estimate the extent of the apparent problem, assuming that only a single failure is the cause of the compliance indication as follows.

2) An estimate of the range of the relative failure rate can be found, based on the number of contacts through which current is observed to flow and not flow. The relative failure rate is simply the inverse of the number of contacts through which current should flow. If compliance is not indicated for V_{11} or V_{21}, current flows through all 170 contacts without failure. If compliance is indicated for a V_{x1} value, the failure rate is at least 1/170, or 0.00588. Compliance readings for the V values indicate the failure rates shown:

Compliance limit found for	Number of contacts in failed chain	Minimum Failure Rate
no Vs	0	0.00
V_{x1}	170	0.00588
V_{x2}	12	0.085
V_{x3}	4	0.250

Note that, while it is possible to make measurements for chains of 158 and 166 contacts, the failure rates that would result are the same order of magnitude as for the 170 contact chain. Making such additional measurements would provide little added information, especially since this design is not intended to locate failures. The computed failure rates should be interpreted qualitatively to indicate that, at best: step coverage is not a problem, may be a problem, or is definitely a problem.

3) Compare the V_{1x} values to the V_{2x} values to assess horizontal vs vertical orientation effects.

REFERENCES

1) Buehler, M. G., The Use of Electrical Test Structure Arrays for Integrated Circuit Process Evaluation, *J. Electrochem. Soc.* **127 (10)**, 2284-2290 (1980).

B.6 Interconnect Resistor

PURPOSE

To determine the load resistance associated with a contact.

APPLICATION

To provide the load resistance of a contact type to a circuit designer.

DESIGN VARIATIONS

See cell names (for contact type):

INTRES_OM_4	(ohmic-to-mesa)
INTRES_M1O_4	(metal 1-to-ohmic)
INTRES_M1R_4	(metal 1-to-resistor)

LAYOUT CONSTRAINTS

These constraints apply to the design shown in figure B-7.

1) Each cell includes two sets of 2 x 2 probe pads, with two contacts between each set. Each contact contains the same two layers. The upper set of pads contains horizontal contacts and the lower vertical contacts, with the current and voltage taps rotated counterclockwise from those in the upper set. (Measuring two such orientations enables the analysis of orientation effects; it also has long use as a measurement technique to eliminate the effects of any offsets in the measurement system.)

2) Each contact is square, is of the minimum-design width, and has taps the same width as the contact edge (to eliminate parasitic resistances due to current crowding as current passes from the taps to the contact). Use minimum-design spacing between contacts. The contacts are separated by the minimum-design spacing. Only the minimum-design widths and spacings are implemented.

METHOD

1) Perform this validation procedure and then use the measurement procedure in 2) below to collect full-wafer data. This validation procedure assures that a valid test structure measurement can be made.

a. Select a forcing current, I_f, based on process history or other knowledge (1 mA is typical for a MESFET process).

b. Collect and evaluate data from both orientations of the test structure. For each orientation, collect data from at least five sites that are uniformly distributed on the wafer.

For each site, sweep and plot the I-V curve from $-I_f$ to $+I_f$. To perform a sweep, force the current from pad 1 to pad 4 on the horizontal orientation (pads 1 and 2 on the vertical orientation), and measure the voltage at pad 2 with respect to pad 1 on the horizontal orientation (pads 4 and 3 on the vertical orientation). In the plots for each orientation, observe whether

intres_m1r_4

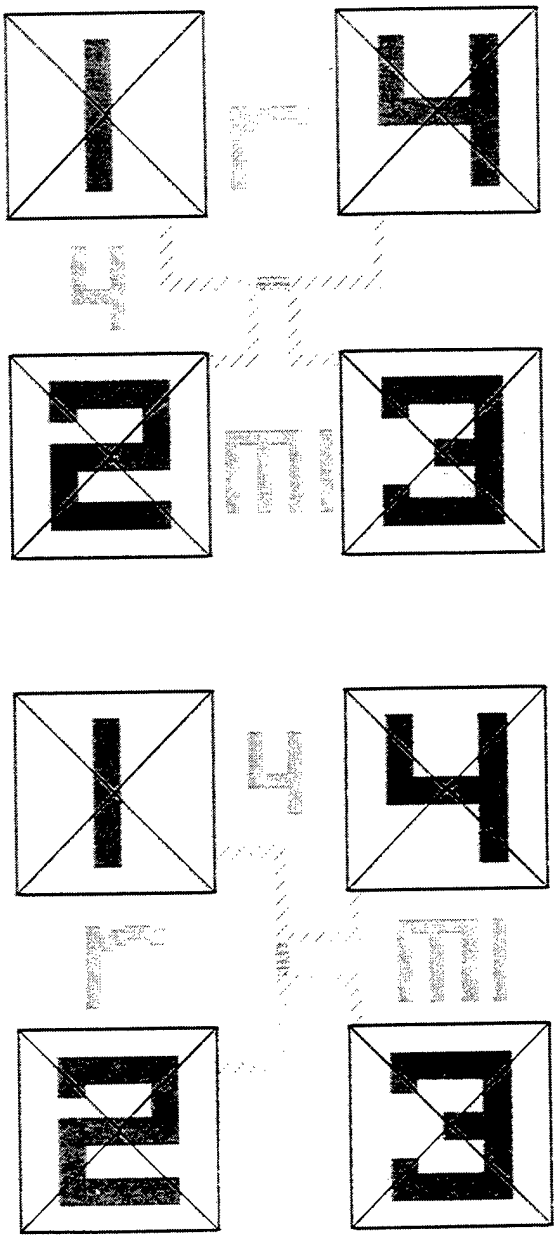


Figure B-7. Interconnect Resistor.

linear operation exists and the curves are approximately centered near 0 V.

If the curves are linear and approximately centered, proceed to 2) and use the I_f just evaluated to perform the measurement procedure for the same design layer variation.

If the curves are not linear and approximately centered, the cause needs to be determined and resolved before proceeding to 2). Some potential causes may be light or heat from the measurement process, offsets in the measurement system, or problems in the fabrication process. Also, determine if both orientations and all sites provide approximately equivalent results. If not, the cause may need to be resolved before proceeding to 2). Some problems may be resolved by performing additional sweeps at progressively higher, but constrained, currents.

2) Determine the load resistance, R_L, for a contact type:

Force	Measure	Compute
1-4, upper: $+I_f$	2-3, upper: V_{11}	
1-4, upper: $-I_f$	2-3, upper: V_{12}	$R_{L1} = \frac{\lvert V_{11}\rvert + \lvert V_{12}\rvert}{2\lvert I_f\rvert}$
1-2, lower: $+I_f$	4-3, lower: V_{21}	
1-2, lower: $-I_f$	4-3, lower: V_{22}	$R_{L2} = \frac{\lvert V_{21}\rvert + \lvert V_{22}\rvert}{2\lvert I_f\rvert}$
		$R_L = \frac{R_{L1} + R_{L2}}{2}$

ANALYSIS OF RESULTS

1) For each site, validate the data as follows. Compare the pairs of V values for a given orientation: V_{11} and V_{12} (horizontal orientation); and V_{21} and V_{22} (vertical orientation). If the compared magnitudes are not approximately equal, the cause should be determined. Compare the R_{L1} and R_{L2} values. If they are not approximately equal, this indicates possible orientation effects. Such possibilities should be investigated by analyzing equivalent-orientation data from other test structures and devices on the wafer.

REFERENCES

1) None.

B.7 Cross-Bridge Resistor

PURPOSE

To determine sheet resistance and linewidth of a conducting layer.

APPLICATION

To assess the quality of a conducting layer.

The cross-bridge resistor provides two critical parameters which can be used in process control or evaluation of lithography tool performance. In either application, the variations in sheet resistance and linewidth across the wafer are compared with predetermined tolerances to assess whether adequate control is maintained.

The cross-bridge resistor has been used extensively to provide precise, fast, and easily-made measurements. Many design variations with respect to cross, bridge, and tap dimensions are possible. The designs provided minimize design-induced errors for linewidth results to less than 20 nm for the 4 μm design and less than 2 nm for the 1 μm design. For further detail on dimensions, uncertainties, and design requirements for a test structure to measure sub-micrometer linewidths, see Reference 1 at the end of this chapter.

DESIGN VARIATIONS

See cell names (for mask layer types):

CROSSBR_M_4	(mesa)
CROSSBR_O_4	(ohmic)
CROSSBR_R_4	(resistor)
CROSSBR_G_1	(gate)
CROSSBR_M1_4	(metal 1)
CROSSBR_T_4	(thick metal)

LAYOUT CONSTRAINTS

These constraints apply to the design shown in figure B-8.

1) Each cell includes a set of 2 x 3 probe pads and a cross-bridge resistor that meets the minimum-design geometries specified in cross-bridge Reference 2. Each cross-bridge design includes a van der Pauw cross (pads 1, 2, 5, and 6) for measuring sheet resistance and a bridge resistor (pads 1, 3, 4, and 5) for measuring linewidth.

2) The bridge and all taps are the minimum-design width for the layer of interest. The length of the bridge (between pads 4 and 5) is $L = 125$ μm.

3) The arms of the van der Pauw cross must have a length ≥ 2 times their width. The van der Pauw width, W_c (dimension of one edge of the square "boxed" area of the cross), must be at least 10 μm. The W_c value is 10 μm in each design except the gate design, where it is 11 μm.

crossbr_t_4

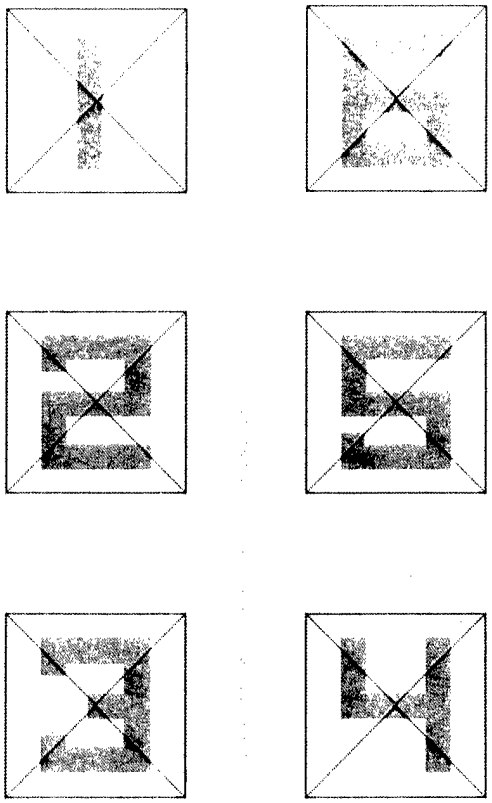


Figure B-8. Cross-Bridge Resistor.

METHOD For some layers, the largest current that can be forced safely produces a small voltage that is measured accurately only if using a voltmeter with nanovolt resolution and teraohm input impedance.

For each design variation, perform the validation procedure in 1) below and then use the measurement procedure starting at 2) below to collect the intended test structure data. The validation procedure determines the forcing current to be used in the measurement procedure and assures that a valid test structure measurement can be made.

1) Determine the appropriate forcing current, I_f, needed to measure the sheet resistance, R_{sh}. This procedure requires considering the current density of the process layer and the resolution of the voltmeter, making some preliminary measurements, and assuring that certain conditions are met. If such a determination has never been made, or the fabrication process has changed since the previous determination, perform the following procedure; otherwise, proceed to the measurement procedure in 2).

a. Determine the (theoretical) maximum I_f that can be applied without Joule heating by considering the maximum normalized current that can be sustained by the layer in the given design variation. For example, consider a gate layer where the maximum normalized current is 9 mA/μm. For a gate cross with W_c = 11 μm, this means an I_f = 50 mA gives an effective normalized current of 4.5 mA/μm, or 50 % of the 9 mA/μm constraint, while an I_f = 99 mA gives 100 %.

To assure that Joule heating is avoided, limit an initial test value for I_f to a value significantly less than the constraint. Also consider any process history and knowledge about the minimum measurable and maximum sustainable currents for the particular layer types. An automated sequence of sweeps (e.g., from 50 % to 80 % of the constraint value) may be helpful in determining the I_f that best satisfies the criteria below, as several tests may be needed to assure these conditions exist.

Note: the I_f must also create sufficient voltage in the cross for an accurate voltage measurement. The minimum voltage needed is in the decade that is 100 times the resolution of the meter. If a differential voltmeter with a resolution of 40 μV is used, the minimum voltage needed is 1 mV. If the target value for R_{sh} for gate metal is 0.03, the minimum I_f that can be used, $I_{fmin} = \frac{V_{min}}{R_{sh}} \cdot \frac{\pi}{\ln 2}$, is 151 mA. This creates a normalized current of 13.7 mA/μm, which exceeds the 9 mA/μm constraint. However, if a voltmeter with a resolution of 10 nV is used, a smaller minimum voltage of 1 μV is needed; the safe I_f = 50 mA cited above creates 330 μV in the cross, which can be accurately measured with this voltmeter.

b. Collect and evaluate data from the cross area of at least five sites that are uniformly distributed on the wafer.

For each site, sweep and plot the I-V curve from $-I_f$ to $+I_f$. To perform a sweep, force the current from pad 6 to pad 1, and measure the voltage at pad 5 with respect to pad 2; this represents the 0° measurement. For the 90° measurement, force the current from pad 1 to pad 2, and measure the voltage at pad 6 with respect to pad 5. In the plots for each measurement orientation, observe whether linear operation exists and the curves are approximately centered near 0 V.

If the curves are linear and approximately centered, proceed to 2) and use the I_f just evaluated to perform the measurement procedure for the same design layer and size variation.

If the curves are not linear and approximately centered, the cause needs to be determined and resolved before proceeding to 2). Some potential causes may be light or heat from the measurement process, offsets in the measurement system, or problems in the fabrication process. Also, check if both orientations at a site and for all sites provide approximately equivalent results. If not, the cause may need to be resolved before proceeding to 2). Some problems may be resolved by performing additional sweeps at progressively higher, but constrained, currents.

2) Determine the sheet resistance, R_{sh}, of a given layer:

Force	Measure	Compute
6-1: $+I_f$	5-2: V_1	$R_1 = \left\|\frac{V_1}{I_f}\right\|$
6-1: $-I_f$	5-2: V_2	$R_2 = \left\|\frac{V_2}{I_f}\right\|$
1-2: $+I_f$	6-5: V_3	$R_3 = \left\|\frac{V_3}{I_f}\right\|$
1-2: $-I_f$	6-5: V_4	$R_4 = \left\|\frac{V_4}{I_f}\right\|$
		$R_{sh1} = \frac{R_1 + R_2}{2}$ $R_{sh2} = \frac{R_3 + R_4}{2}$ $R_{sh} = \frac{\pi}{\ln 2} \cdot \frac{R_{sh1} + R_{sh2}}{2}$

3) Determine the linewidth, W, of a given layer, using the R_{sh} value determined in 2) above:

Force	Measure	Compute
1-3: $+I_f$	5-4: V_1	$R_{1b} = \left\|\frac{V_1}{I_f}\right\|$
1-3: $-I_f$	5-4: V_2	$R_{2b} = \left\|\frac{V_2}{I_f}\right\|$
		$R_b = \frac{R_{1b} + R_{2b}}{2\|I_f\|}$ $W = \frac{R_{sh} L}{R_b}$

ANALYSIS OF RESULTS

1) Compare the R_1 and R_2 values (0° measurement) and compare the R_3 and R_4 values (90° measurement). If the compared magnitudes are not approximately equal, the cause should be determined. Here, V_1 and V_3 should be positive, while V_2 and V_4 should be negative. Compare the R_{sh1} and R_{sh2} values, and if they are not approximately equal, this indicates possible orientation effects. Such possibilities should be investigated by analyzing equivalent-orientation data from other test structures and devices on the wafer.

2) Compare the R_{1b} and R_{2b} values. If the compared magnitudes are not approximately equal, the cause should be determined. Here, V_1 should be positive, while V_2 should be negative.

3) Compare the R_{sh} value to its target value and the W value to the design linewidth.

REFERENCES

1) Linholm, L. W., Allen, R. A., and Cresswell, M. W., Microelectronic Test Structures for Feature Placement and Electrical Linewidth Metrology, in the *Handbook of Critical Dimension Metrology and Process Control*, Vol. CR52, K. M. Monahan, Ed. (SPIE, Bellingham, WA, 1994), pp. 91-118.

2) Buehler, M. G., and Hershey, C. W., The Split-Cross-Bridge Resistor for Measuring the Sheet Resistance, Linewidth, and Line Spacing of Conducting Layers, *IEEE Trans. Electron Devices* **ED-33** (10), 1572-1579 (1986).

3) Carver, G. P., Mattis, R. L., and Buehler, M. G., Design Considerations for the Cross-Bridge Sheet Resistor, NBSIR 82-2548 (1982).

4) Buehler, M. G., Grant, S. D., and Thurber, W. R., Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers, *J. Electrochem. Soc.* **125** (4), 650-654 (1978).

5) Buehler, M. G., and Thurber, W. R., An Experimental Study of Various Cross Sheet Resistor Test Structures, *J. Electrochem. Soc.* **125** (4), 645-650 (1978).

6) David, J. M., and Buehler, M. G., A Numerical Analysis of Various Cross Sheet Resistor Test Structures, *Solid-State Electronics* **20**, 539-543 (1977).

7) Troccolo, P., Mantalas, L., Allen, R. A., and Linholm L. W., Extending Electrical Measurements to the 0.5 μm Regime, Proceedings of the SPIE, International Society for Optical Engineering, *Integrated Circuit Metrology, Inspection, and Process Control V* **1464**, 90-103 (1991).

B.8 MIMIC-Standard 200 μm FET

PURPOSE To determine dc FET parameters.

APPLICATION To enable device and circuit designers to assess FET performance.

DESIGN VARIATIONS See cell names:

RFFETH_1X200 and RFFETV_1X200

The "H" or "V" following "RFFET" denotes the different designs that enable the horizontal and vertical FET orientations to be probed with the same probing procedure and without rotating the wafer.

LAYOUT CONSTRAINTS These constraints apply to the designs shown in figures B-9 and B-10.

1) Each cell includes a set of 2 x 3 probe pads and a FET. Each FET has a 1 μm gate length and a 200 μm gate width, as indicated by the "1X200" in its cell name. The gate is centered in a channel in the 5 μm space between the source and drain. The left three pads are source-gate-source terminals and the right three pads are source-drain-source terminals, to allow on-wafer probing by rf network analyzer test equipment. (Note: this document includes only the dc testing specifications.)

2) The RFFETH cell includes gate metal that is outside the 2 x 6 probe-pad area by 8 μm and 6 μm from the pad 2 and 5 sides, respectively. While any other NISTGAAS cell can be placed adjacent to an RFFETH cell without violating any design rule, the user needs to assure that this is also true if placing non-NISTGAAS constructs adjacent to this cell.

METHOD Determine these dc FET parameters for each orientation:

dc FET Parameter	Parameter Symbol	Test Number
Saturated source-drain current	I_{dss}	1
Saturation voltage	V_{sat}	2
Pinch-off voltage	V_{po}	3
Source-drain resistance	R_{ds}	4
Drain resistance	R_{d}	5
Source resistance	R_{s}	6
Transconductance	g_{m}	7
Source-gate breakdown voltage	V_{rgs}	8
Drain-gate breakdown voltage	V_{rdg}	9

rffeth_1x200

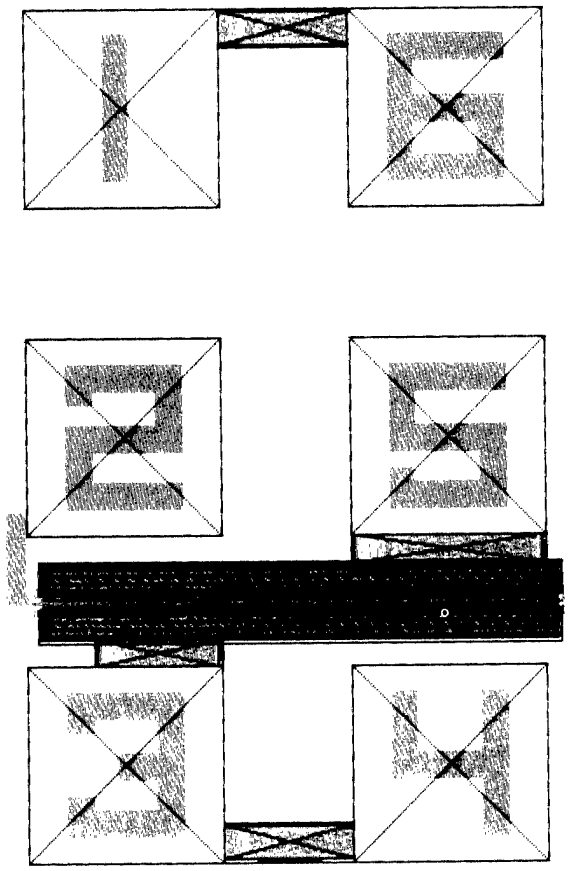


Figure B-9. MIMIC-Standard 200 μm FET (Horizontal).

rffetv_1x200

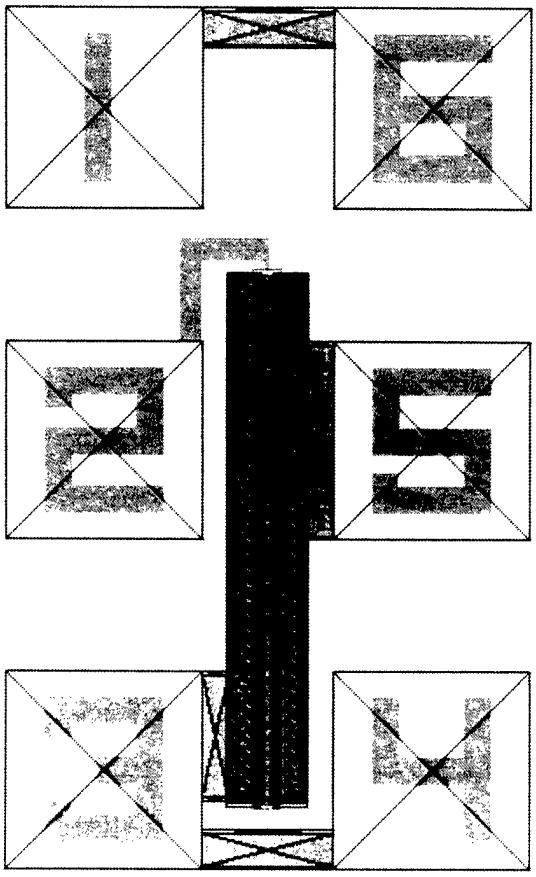


Figure B-10. MIMIC-Standard 200 μm FET (Vertical).

1) For some of the tests specified on the next sheet, a preliminary characterization procedure is needed before full-wafer data is collected to assure that valid measurements can be made. Such tests include a parenthetical note referencing a circled number that is found on the subsequent page.

If the procedure following the note has never been performed, or the fabrication process has changed since the previous characterization, perform the "Preliminary characterization" portion before using the "Post-characterization" portion.

In general, the preliminary characterization portion involves performing a sweep to demonstrate appropriate operation (i.e., pinch-off or linearity) and to aid in choosing 1 or 2 appropriate forcing values for use in the full-wafer data collection procedure. This approach increases the efficiency of the full-wafer data collection process without ignoring critical validation measurements.

Characterization measurements are made at five sites that are uniformly distributed on the wafer.

In applying these procedures, the user should also consider the following. The procedures reference typical values, which may need to be refined for the user's process. Also, for some parameters, other procedures may provide adequate data. If the user has such procedures which are associated with significant process history, and wants to retain them, the user should demonstrate the two procedures provide equivalent or acceptably accurate data.

2) Execute tests 1-3 on the next sheet. If V_{po} is not within the predetermined limits, further testing is not meaningful; otherwise, continue with tests 4-9.

Note: The equations in the **Compute** column follow the convention established by the International System of Units: $\{A\}_x$ is the numerical value of quantity A when its value is expressed in the unit X.

Test	Force			Measure	Compute
	gate	drain	source		
1	2: $V_g = 0.0$ V	5-3: $V_{ds} = V_1$	3: $V_s = 0.0$ V	5-3: I_{ds}	$\{I_{dss}\}_{mA/mm} = \frac{\{I_{ds}\}_A}{\{W\}_{mm}} 10^3$
2	2: $V_g = 0.0$ V	5-3: $I_{ds} = I_1$	3: $V_s = 0.0$ V	5-3: V_{ds}	$\{V_{sat}\}_V = \{V_{ds}\}_V$
3	2-3: step V_{gs} (see Note ①)	5-3: $V_{ds} = V_1$	3: $V_s = 0.0$ V	5-3: I_{ds} 2-3: V_{gs}	$\{V_{po}\}_V = \{V_{gs} @ I_{ds} = I_2\}_V$
4	2: $V_g = 0.0$ V	5-3: $I_{ds} = I_3$	3: $V_s = 0.0$ V	5-3: V_{ds}	$\{R_{ds}\}_{W \bullet mm} = \frac{\{V_{ds}\}_V}{\{I_{ds}\}_A} \{W\}_{mm}$
5	2-5: step I_{gd} (see Note ②)	5: $V_d = 0.0$ V	3-5: $I_{sd} = I_4$	3-5: V_{sd} 2-5: I_{gd}	$\{R_d\}_{\Omega \bullet mm} = \frac{\{\Delta V_{sd}\}_V}{\{\Delta I_{gd}\}_A} \{W\}_{mm}$
6	2-3: step I_{gs} (see Note ②)	5-3: $I_{ds} = I_4$	3: $V_s = 0.0$ V	5-3: V_{ds} 2-3: I_{gs}	$\{R_s\}_{\Omega \bullet mm} = \frac{\{\Delta V_{ds}\}_V}{\{\Delta I_{gs}\}_A} \{W\}_{mm}$
7	2-3: step V_{gs} (see Note ③)	5: $V_d = V_1$	3: $V_s = 0.0$ V	5-3: I_{ds} at each V_{gs} step	$\{g_m\}_{mS/mm} = \frac{\{\Delta I_{ds}\}_A}{\{\Delta V_{gs}\}_V} \frac{10^3}{\{W\}_{mm}}$
8	2: $V_g = 0.0$ V	5: open	2-3: $I_{gs} = I_5$	2-3: V_{gs}	$\{V_{rgs}\}_V = \{V_{gs}\}_V$
9	2: $V_g = 0.0$ V	5-2: $I_{dg} = I_5$	3: open	5-2: V_{dg}	$\{V_{rdg}\}_V = \{V_{dg}\}_V$

where:

$V_1 = V_{ds} = 2.5$ V or 3.0 V (for typical MESFET process)
W = 200 µm (design value for gate width)
$I_1 = 0.9\ I_{ds}$ value in Test 1
$I_2 = 0.02\ I_{ds}$ value in Test 1
$I_3 = 5$ mA/mm * W mm (for typical MESFET process)
$I_4 = 1$ nA (for typical MESFET process)
$I_5 = 1$ mA/mm * W mm (for typical MESFET process)

Notes:

① Preliminary characterization at each of 5 sites (V_{gs})

a. If the device is a low-noise FET, typical values are V_{gs} = [0.0, -3.0] V and ΔV_{gs} = 0.1 V. At pinch-off, the curve trace of I_{ds} vs V_{ds} will be near I_{ds} = 0 and nearly parallel to the x-axis.

b. If the device is not a low-noise FET or did not pinch-off, use V_{gs} = [0.0, -10.0] V and ΔV_{gs} = 1.0 V. When approximate pinch-off is located, use ΔV_{gs} = 0.1 V between the two integer V_{gs} values to provide a measurement resolution of 0.1 V.

Post-characterization measurement (V_{gs})

Instead of stepping V_{gs} and measuring I_{ds}, force I_{ds} at the value found above, and measure V_{gs}.

② Preliminary characterization at each of 5 sites (R_d, R_s)

a. For I_g, use 5 evenly-spaced points over the range [I_L, I_U], where typical values are I_L = 0.1 mA and I_U = 10.0 mA.

b. Perform a least squares fit and substitute the slope for $\Delta V_d / \Delta I_g$.

Post-characterization measurement (R_d, R_s)

Instead of stepping I_g, force I_g at 2 points: $I_{MID} - I_{INC}$ and $I_{MID} + I_{INC}$, where $I_{MID} = \frac{I_U - I_L}{2}$ and $I_{INC} = \frac{I_U - I_{MID}}{2}$.

③ Preliminary characterization at each of 5 sites (g_m)

a. For V_{gs}, use 5 evenly-spaced points over the range [V_L, V_U] = [$V_N - V_{INC}$, $V_N + V_{INC}$], where typical values are:
for N = 0, find $g_{m(0)}$ [saturation]: $V_N = V_{gs}$ = 0.0 V, V_{INC} = 0.2 V, and ΔV_{gs} = 0.1 V.
for N = 50, find $g_{m(50)}$ [50 % Idss]: $V_N = V_{gs}$ @ 0.5 I_{ds} value in Test 1, V_{INC} = 0.1 V, and ΔV_{gs} = 0.05 V.

b. Perform a least squares fit and substitute the slope for $\Delta I_{ds} / \Delta V_{gs}$.

Post-characterization measurement (g_m)

Instead of stepping V_{gs}, force V_{gs} at 2 points: $V_{MID} - V_{INC}$ and $V_{MID} + V_{INC}$, where $V_{MID} = \frac{V_U - V_L}{2}$ and $V_{INC} = \frac{V_U - V_{MID}}{2}$.

ANALYSIS OF RESULTS

1) If an unacceptable standard deviation exists for a full-wafer data set, the preliminary characterization procedure may need to be performed at all sites to investigate this observation.

2) Measured/computed values should be compared to target values and limits obtained from process simulation or history.

3) Check for possible orientation effects by creating wafer maps of full-wafer data for each dc FET parameter. Orientation effects may be further analyzed by examining possible correlations between the various dc FET parameters and equivalent-orientation data from other test structures and devices on the wafer.

REFERENCES

Williams, R., *Modern GaAs Processing Methods* (Artech House, Norwood, MA, 1990), pp. 345-355.

Appendix C - NISTGAAS Test Structure Sideviews

Appendix C - NISTGAAS Test Structure Sideviews

The following process sideviews correspond to the checkplots provided in Appendix B. Each sideview is taken from a horizontal slice through the contact(s) or construct(s) where measurements are made. Since this slice is the same regardless of the orientation of a given test structure type, sideviews are shown for only a single orientation of the test structure type. The layer thicknesses depicted in each sideview are not precisely to scale (per the process shown in figure 2) because of the range of magnitudes represented. However, the thicknesses shown do reflect realistic relative differences between all layers except the resistor layer, which is much thinner than is (relatively) shown.

conres_m1r_10

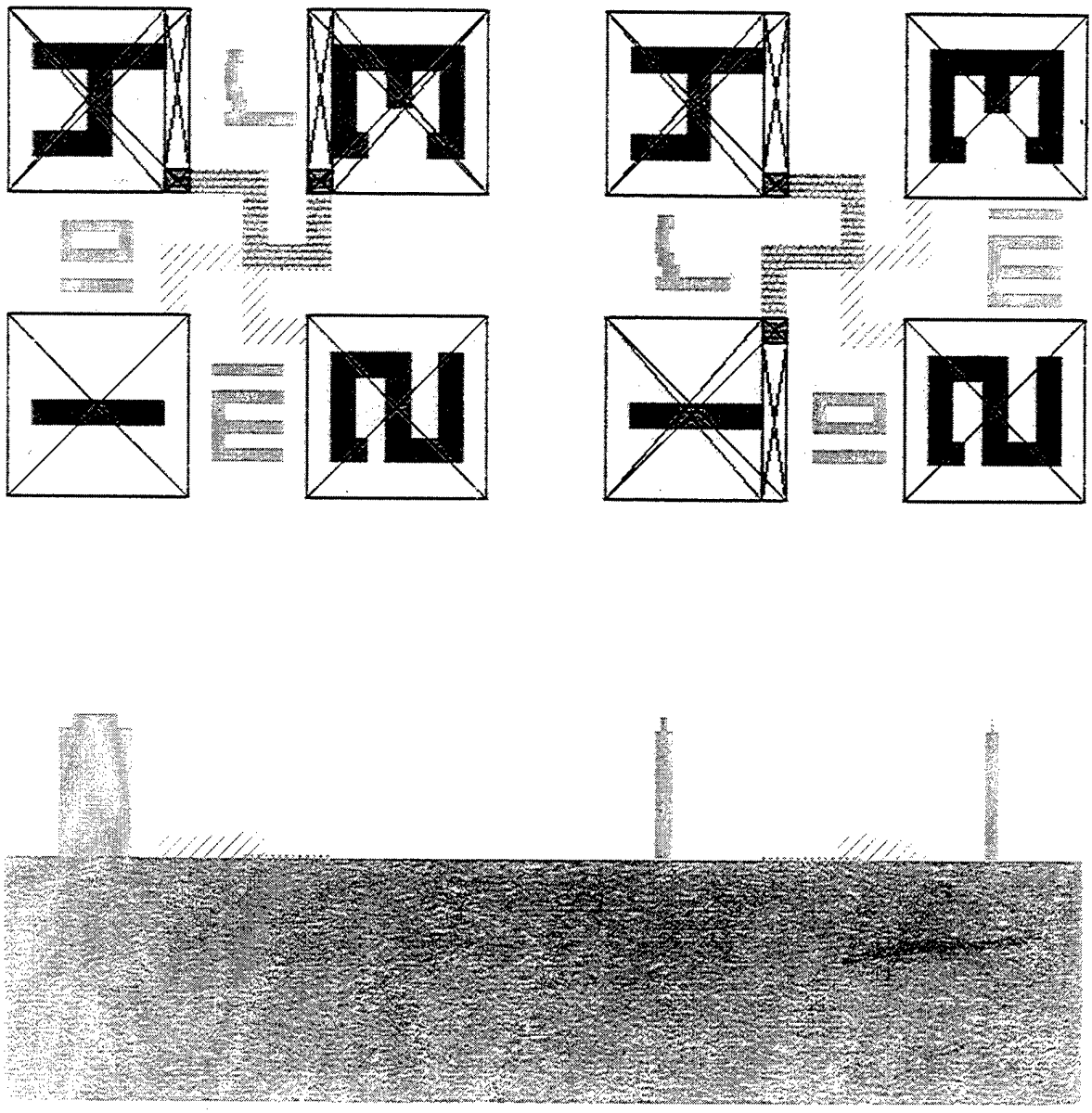


Figure C-1. Sideview: Kelvin-Cross Interfacial Contact Resistor (Four-Pad).

conressh_o_10

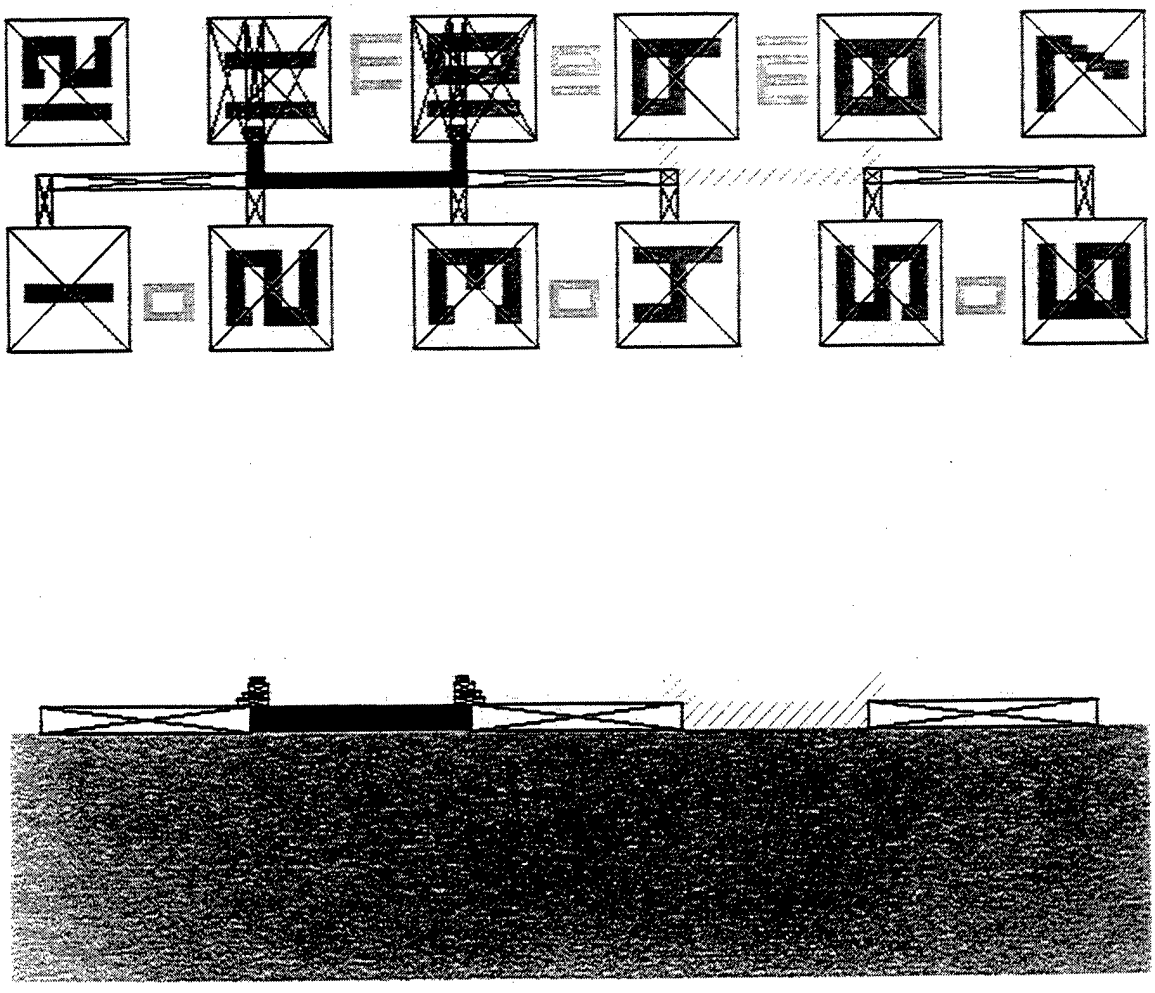


Figure C-2. Sideview: Kelvin-Cross Interfacial Contact Resistor (Shared-Pad).

alignv_go_4

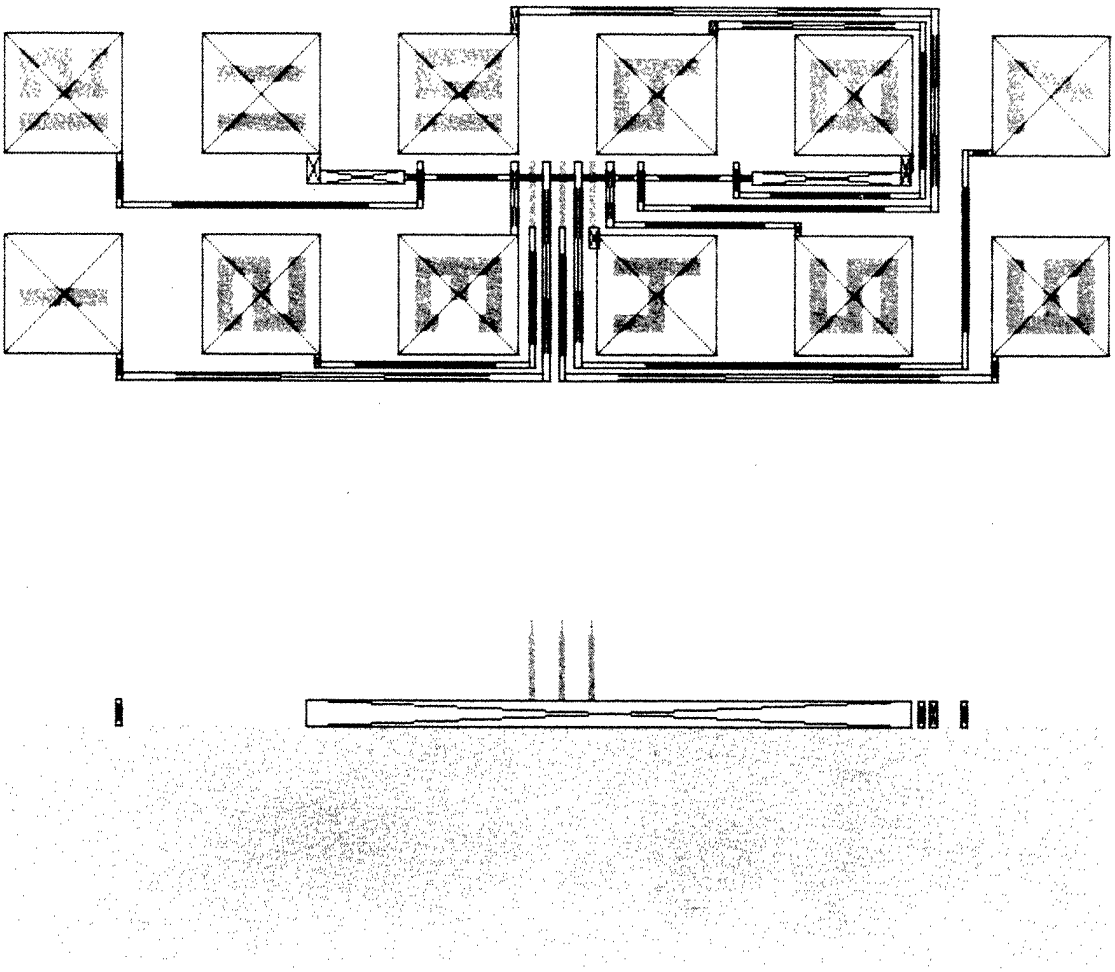


Figure C-3. Sideview: Nanometer-Resolution Alignment Structure .

vpauw_m_12

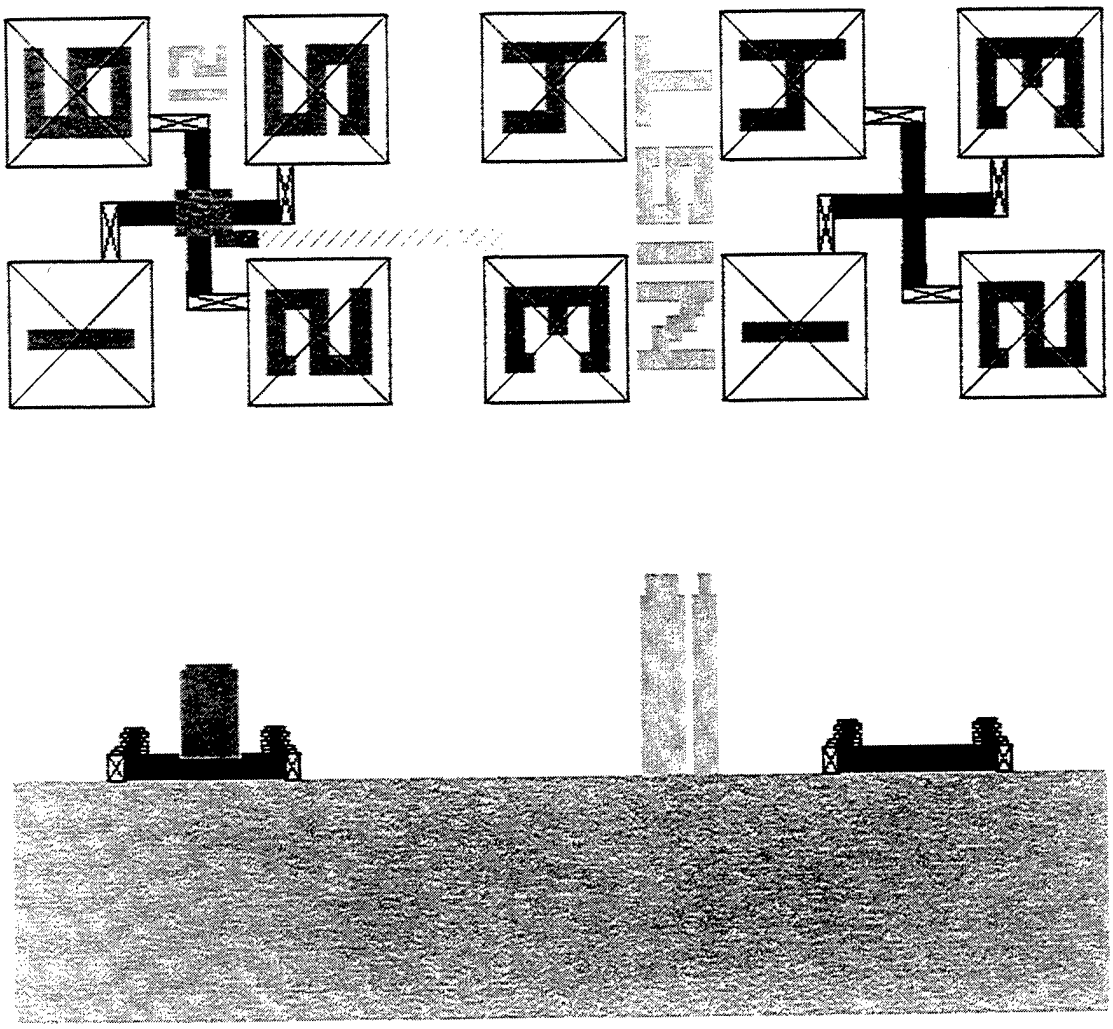


Figure C-4. Sideview: Mesa/Channel van der Pauw Sheet Resistor.

meander_m1g_4

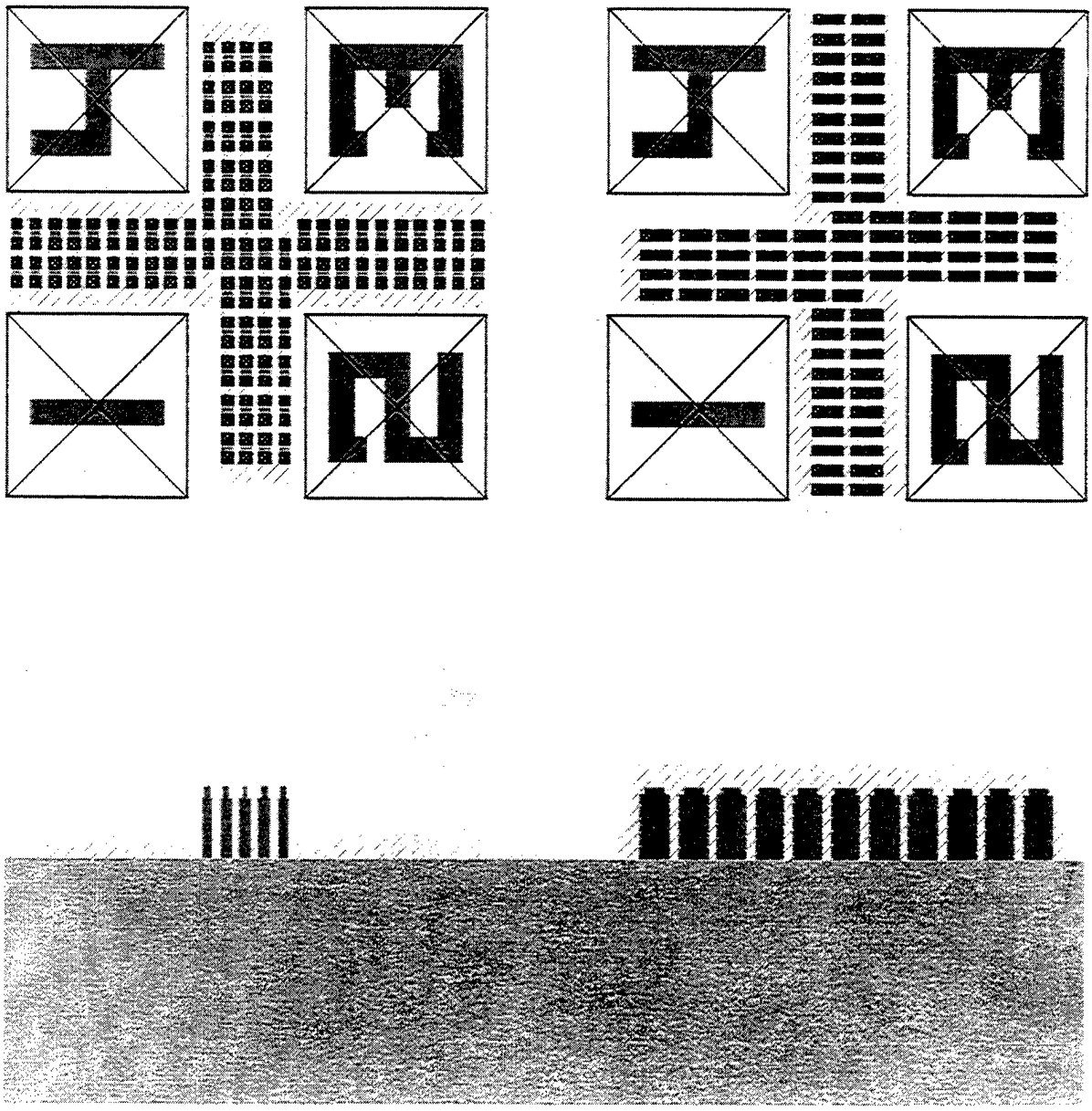


Figure C-5. Sideview: Step Coverage/Interconnect Meander.

intres_m1r_4

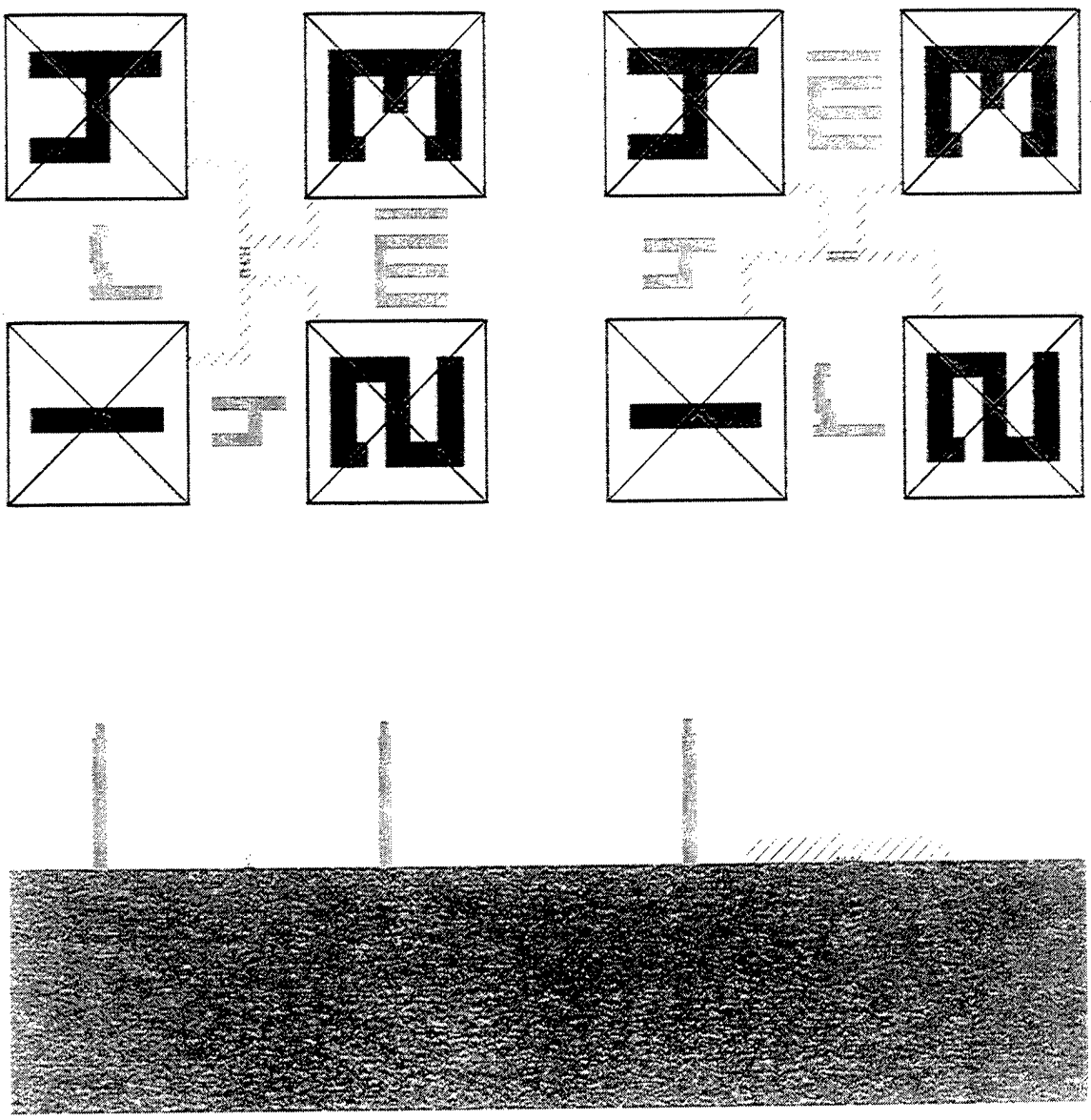


Figure C-6. Sideview: Interconnect Resistor.

crossbr_t_4

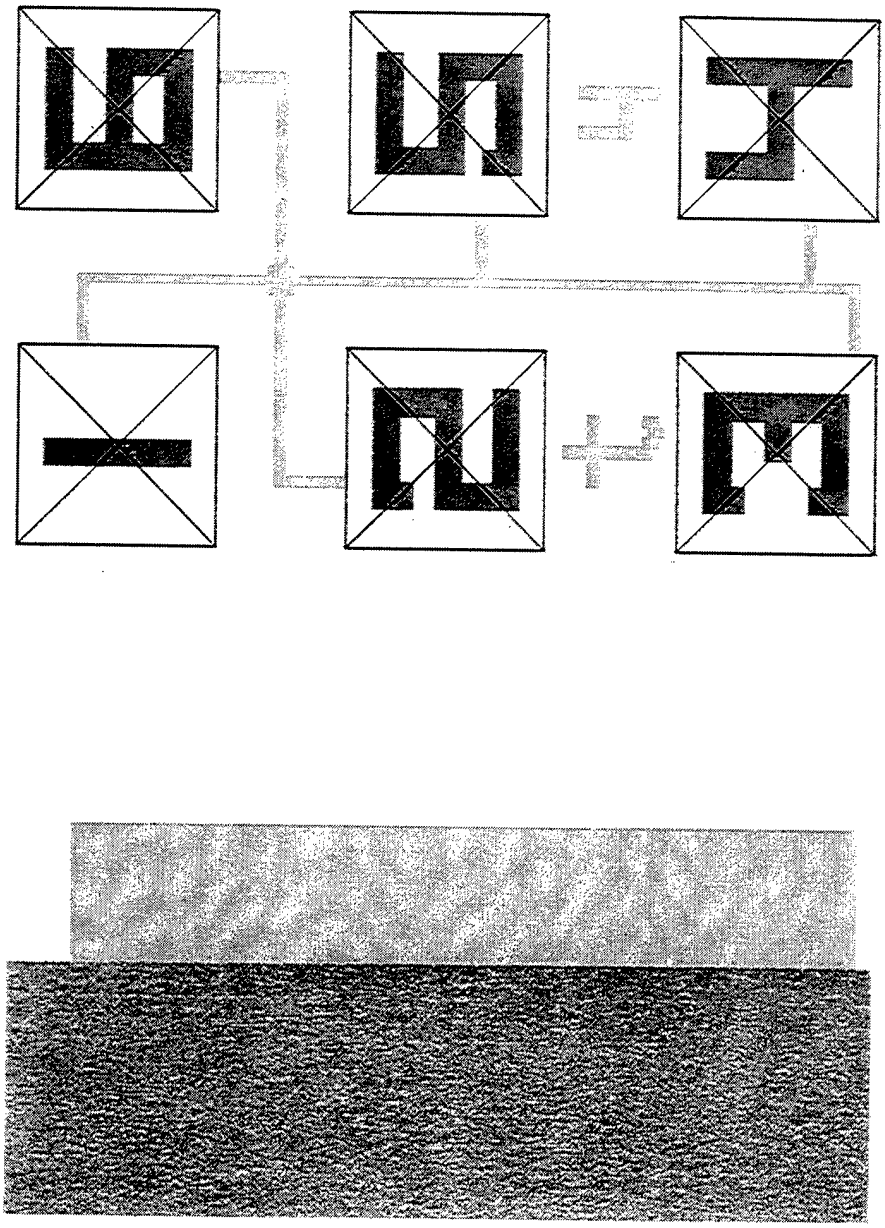


Figure C-7. Sideview: Cross-Bridge Resistor.

rffeth_1x200

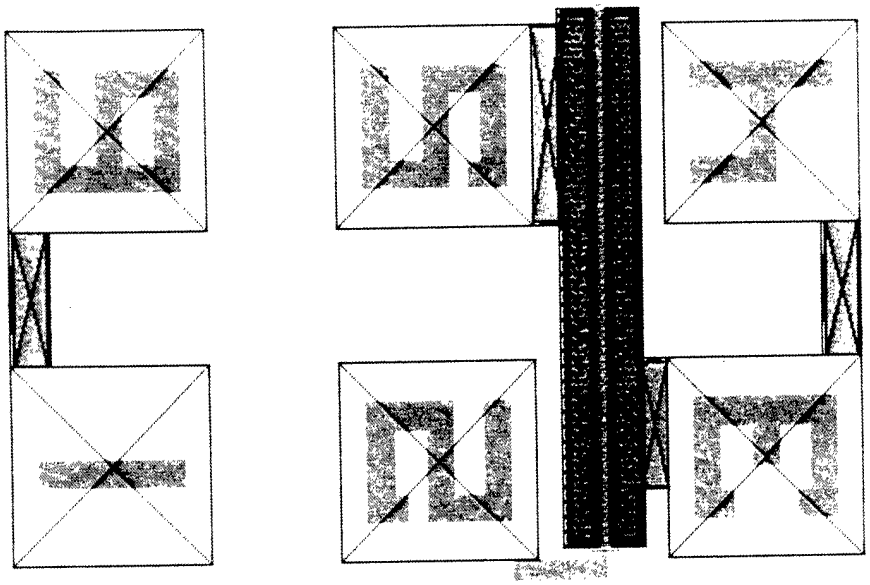


Figure C-8. Sideview: MIMIC-Standard 200 μm FET.

NIST Technical Publications

Periodical

Journal of Research of the National Institute of Standards and Technology—Reports NIST research and development in those disciplines of the physical and engineering sciences in which the Institute is active. These include physics, chemistry, engineering, mathematics, and computer sciences. Papers cover a broad range of subjects, with major emphasis on measurement methodology and the basic technology underlying standardization. Also included from time to time are survey articles on topics closely related to the Institute's technical and scientific programs. Issued six times a year.

Nonperiodicals

Monographs—Major contributions to the technical literature on various subjects related to the Institute's scientific and technical activities.

Handbooks—Recommended codes of engineering and industrial practice (including safety codes) developed in cooperation with interested industries, professional organizations, and regulatory bodies.

Special Publications—Include proceedings of conferences sponsored by NIST, NIST annual reports, and other special publications appropriate to this grouping such as wall charts, pocket cards, and bibliographies.

National Standard Reference Data Series—Provides quantitative data on the physical and chemical properties of materials, compiled from the world's literature and critically evaluated. Developed under a worldwide program coordinated by NIST under the authority of the National Standard Data Act (Public Law 90-396). NOTE: The Journal of Physical and Chemical Reference Data (JPCRD) is published bimonthly for NIST by the American Chemical Society (ACS) and the American Institute of Physics (AIP). Subscriptions, reprints, and supplements are available from ACS, 1155 Sixteenth St., NW, Washington, DC 20056.

Building Science Series—Disseminates technical information developed at the Institute on building materials, components, systems, and whole structures. The series presents research results, test methods, and performance criteria related to the structural and environmental functions and the durability and safety characteristics of building elements and systems.

Technical Notes—Studies or reports which are complete in themselves but restrictive in their treatment of a subject. Analogous to monographs but not so comprehensive in scope or definitive in treatment of the subject area. Often serve as a vehicle for final reports of work performed at NIST under the sponsorship of other government agencies.

Voluntary Product Standards—Developed under procedures published by the Department of Commerce in Part 10, Title 15, of the Code of Federal Regulations. The standards establish nationally recognized requirements for products, and provide all concerned interests with a basis for common understanding of the characteristics of the products. NIST administers this program in support of the efforts of private-sector standardizing organizations.

Order the **following** *NIST publications—FIPS and NISTIRs—from the National Technical Information Service, Springfield, VA 22161.*

Federal Information Processing Standards Publications (FIPS PUB)—Publications in this series collectively constitute the Federal Information Processing Standards Register. The Register serves as the official source of information in the Federal Government regarding standards issued by NIST pursuant to the Federal Property and Administrative Services Act of 1949 as amended, Public Law 89-306 (79 Stat. 1127), and as implemented by Executive Order 11717 (38 FR 12315, dated May 11, 1973) and Part 6 of Title 15 CFR (Code of Federal Regulations).

NIST Interagency Reports (NISTIR)—A special series of interim or final reports on work performed by NIST for outside sponsors (both government and nongovernment). In general, initial distribution is handled by the sponsor; public distribution is by the National Technical Information Service, Springfield, VA 22161, in paper copy or microfiche form.